TD99102 - Die Specifications

UltraCMOS® High-speed FET and GaN Transistor Driver, 20 MHz

Product Specification

Features

- TID = 100 krad(Si)
- SEL Immune
- High- and Low-side FET drivers
- Dead-time control
- Fast propagation delay, 9 ns
- Tri-state enable mode
- Sub-nanosecond rise and fall time
- 2 A / 4 A peak source/sink current
- Bumped flip chip die

Applications

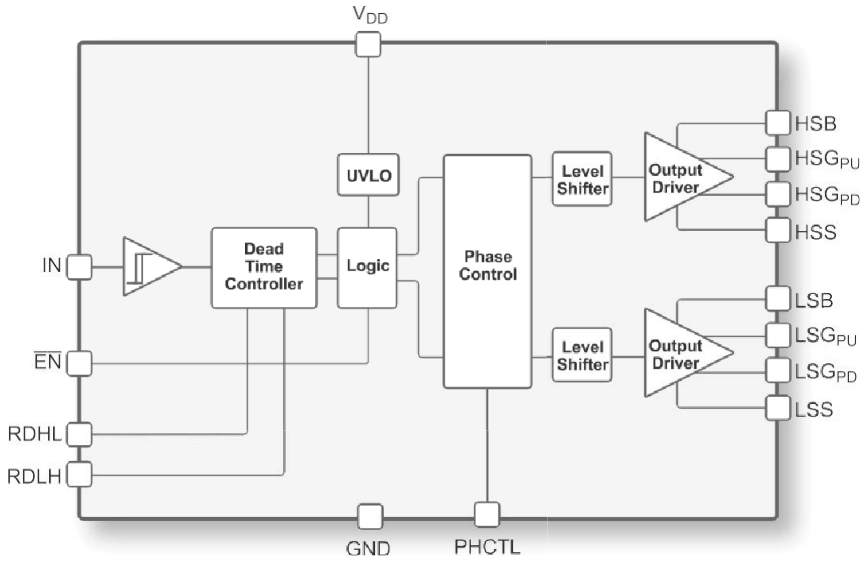
- dc–dc conversions
- ac–dc conversions
- Orbital Point of Load (POL) module power distribution
- Motor driver

Product Description

The TD99102 is an integrated high-speed driver designed to control the gates of external power devices such as enhancement mode gallium nitride (GaN) High Electron Mobility Transistor (HEMT) and power MOSFETs. The outputs of the TD99102 are capable of providing switching transition speeds in the sub-nanosecond range for switching applications up to 20 MHz. The TD99102 is optimized for matched dead time and offers best-in-class propagation delay to improve system bandwidth. High switching speeds result in smaller peripheral components and enable innovative designs for high reliability orbital motor driver and POL applications. The TD99102 is available as a bumped flip chip die to enable minimum design footprint required for high speed switching power applications.

The TD99102 is manufactured on Peregrine's UltraCMOS® process, a patented advanced form of silicon-on-insulator (SOI) technology, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1 • *Functional Diagram* ***TD99102***



Product Description (cont.)

The TD99102 operates from 4 V to 6.5 V and can support a high side floating supply voltage of 60 V. An optional internal synchronous bootstrap circuit limits overcharging of the bootstrap capacitor during reverse body diode conduction, preventing the GaN FETs from exceeding their maximum gate-to-source voltage rating. The TD99102 also features a dead-time controller that allows timing of the LS and HS gates to eliminate any large shoot-through currents that could dramatically reduce the efficiency of the circuit and potentially damage the transistors.

The TD99102 is available as a flip chip die and is manufactured on the UltraCMOS process, a patented advanced form of silicon-on-insulator (SOI) technology, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for* ***TD99102***

	Min	Max	Unit
Low-side bias (LSB) to low-side source (LSS)	–0.3	7	V
High-side bias (HSB) to high-side source (HSS)	–0.3	7	V
Input signal	–0.3	7	V
HSS to LSS	–100	100	V
HSS to GND	-1	100	V
LSS to GND	-1	100	V
ESD voltage HBM(*), all pins		500	V
Note: * Human body model (MIL-STD 883 Method 3015).			

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the TD99102. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • *Recommended Operating Conditions for* ***TD99102***

Parameter	Min	Typ	Max	Unit
Supply for driver front-end, V_{DD}	4.0	5.0	6.0	V
Supply for high-side driver, HSB	4.0	5.0	6.0	V
Supply for low-side driver, LSB	4.0	5.0	6.0	V
Logic HIGH for control input	1.6		6.0	V
Logic LOW for control input	0		0.6	V
HSS range	0		60	V
LSS range	0		60	V
Operating temperature	–40		+105	°C
Junction temperature	–40		+125	°C

Electrical Specifications

Table 3 provides the key electrical specifications @ -40 °C to +105 °C, V_{DD} = 5V, 100 pF load unless otherwise specified; RDHL and RDLH are ±1% tolerance unless otherwise specified.

Table 3 • *dc Characteristics*

Parameter	Condition	Min	Typ	Max	Unit
dc Characteristics					
V_{DD} quiescent current	V_{DD} = 5 V		1.3		mA
HSB quiescent current	V_{DD} = 5 V		2.7		mA
LSB quiescent current	V_{DD} = 5 V		2.7		mA
Total quiescent current	V_{DD} = 5 V		6.7	9.0	mA
V_{DD} quiescent current	V_{DD} = 6 V		1.6		mA
HSB quiescent current	V_{DD} = 6 V		3.6		mA
LSB quiescent current	V_{DD} = 6 V		3.6		mA
Total quiescent current	V_{DD} = 6 V		9.0	11.6	mA

Notes: These limits are derived from a limited sample and are not production tested.

Table 3 • *dc/ac Characteristics (Cont.)*

Parameter	Condition	Min	Typ	Max	Unit
Under Voltage Lockout					
Under voltage release (rising)			3.6	4	V
Under voltage hysteresis			400		mV
Gate Drivers					
HSG_{PU}/LSG_{PU} pull-up resistance			1.9		Ω
HSG_{PD}/LSG_{PD} pull-down resistance			1.3		Ω
HSG_{PU}/LSG_{PU} leakage current	HSB–HSG_{PU} = 5V, LSB–LSG_{PU} = 5V		10		µA
HSG_{PD}/LSG_{PD} leakage current	HSG_{PD}–HSS = 5V, LSG_{PD}–LSS = 5V		10		µA
Dead-time Control					
Dead-time control voltages	HSB=LSB, 80.6 kΩ resistor to GND		1.3		V
Dead-time from HSG going low to LSG going high	RDHL = 30 kΩ, CL 1,000 pF load		1.9		ns
	RDHL = 80.6 kΩ, CL 1,000 pF load		7.0		ns
	RDHL = 150 kΩ, CL 1,000 pF load		13.6		ns
	RDHL = 255 kΩ, CL 1,000 pF load		23.5		ns
Dead-time from LSG going low to HSG going high	RDLH = 30 kΩ, CL 1,000 pF load		1.8		ns
	RDLH = 80.6 kΩ, CL 1,000 pF load		6.7		ns
	RDHL = 150 kΩ, CL 1,000 pF load		13.2		ns
	RDHL = 255 kΩ, CL 1,000 pF load		22.7		ns
Switching Characteristics					
LSG turn-off propagation delay	VCC = 5 V with 255 kΩ resistor to GND		9.1		ns
HSG rise time	10%–90% with 1,000 pF load		3.0		ns
LSG rise time	10%–90% with 1,000 pF load		3.0		ns
HSG fall time	10%–90% with 1,000 pF load		4.0		ns
LSG fall time	10%–90% with 1,000 pF load		5.0		ns
Minimum output pulse width	RDLH = RDLH = 30 kΩ, CL 1,000 pF load		2.0	5.0	ns
Max switching frequency @ 50% duty cycle	RDHL = RDLH = 80.6 kΩ, CL 1,000 pF load	40			MHz

Control Logic

Table 4 provides the control logic truth table for the TD99102

Table 4 • *Truth Table for* ***TD99102***

$\overline{EN}$	IN	HSGPU–HSS	HSGPD–HSS	LSGPU–LSS	LSGPD–LSS
L	L	Hi–Z	L	H	Hi–Z
L	H	H	Hi–Z	Hi–Z	L
H	L	Hi–Z	L	Hi–Z	L
H	H	Hi–Z	L	Hi–Z	L

Typical Performance Data

Figure 2–**Figure 4** show the typical performance data @ +25 °C, V_{DD} = 5 V, load = 2.2 Ω resistor in series with 100 pF capacitor, HSB and LSB bootstrap diode included, unless otherwise specified.

Figure 2 • *Quiescent Current vs Temperature*

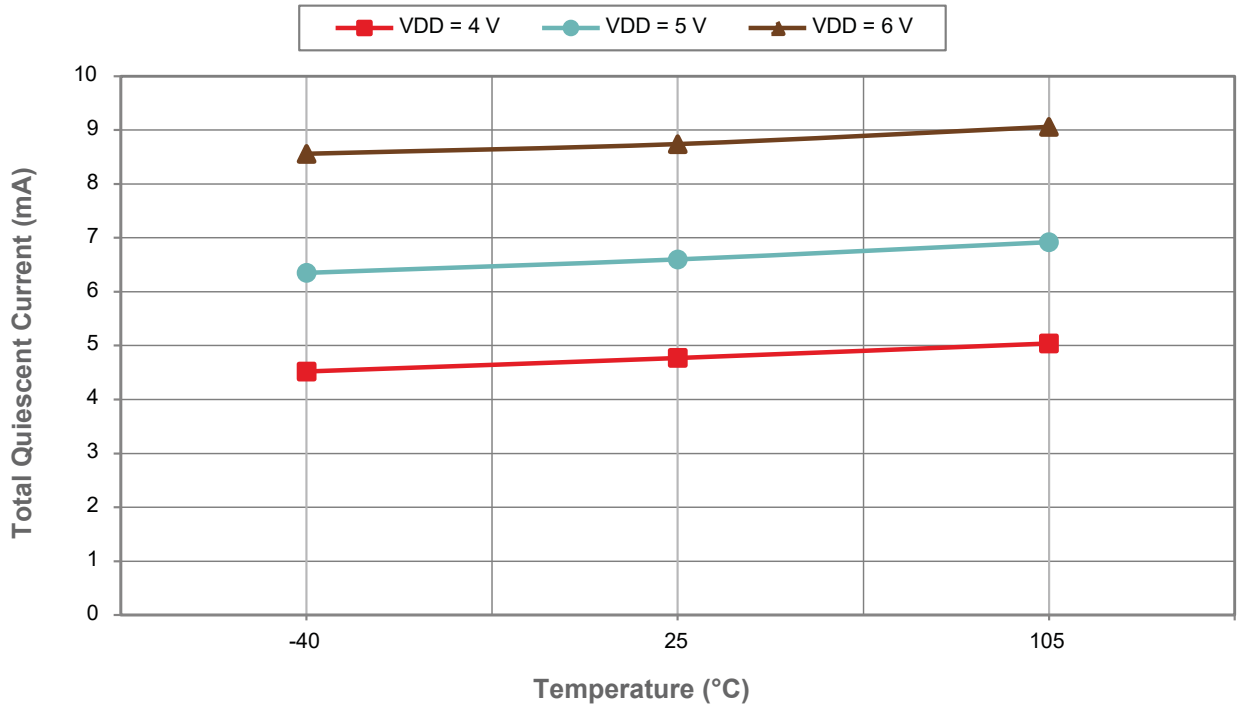


Figure 3 • *UVLO Threshold vs Temperature*

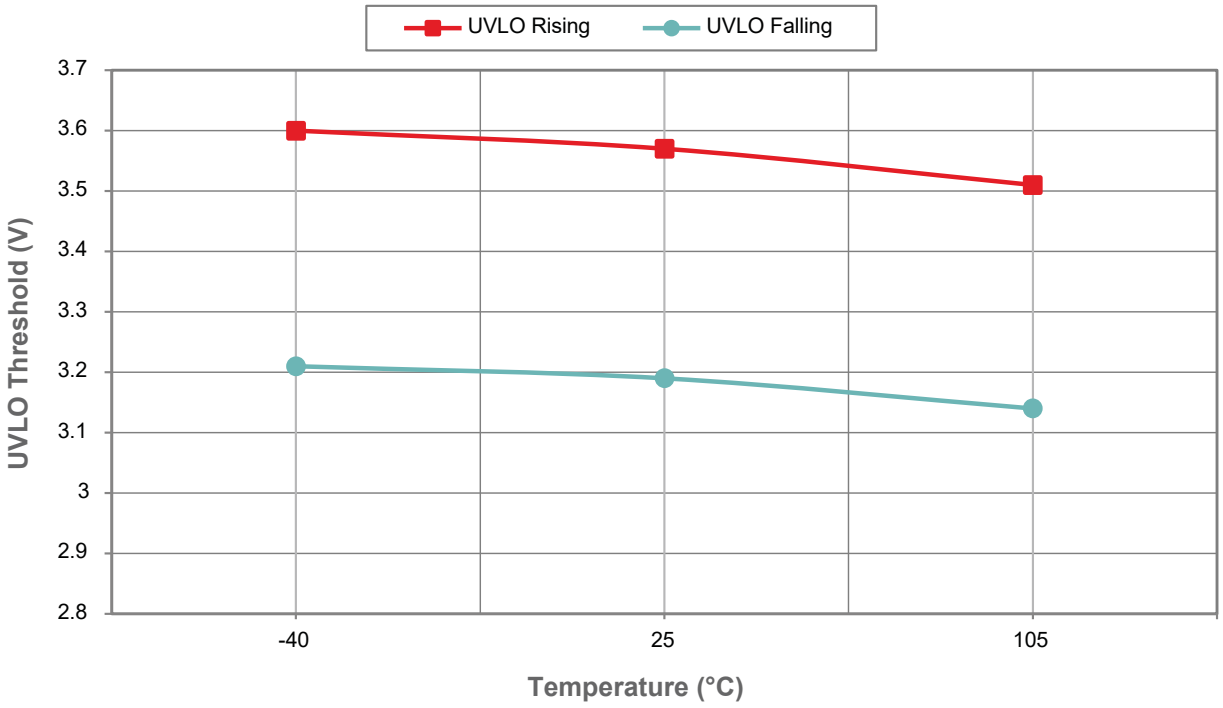
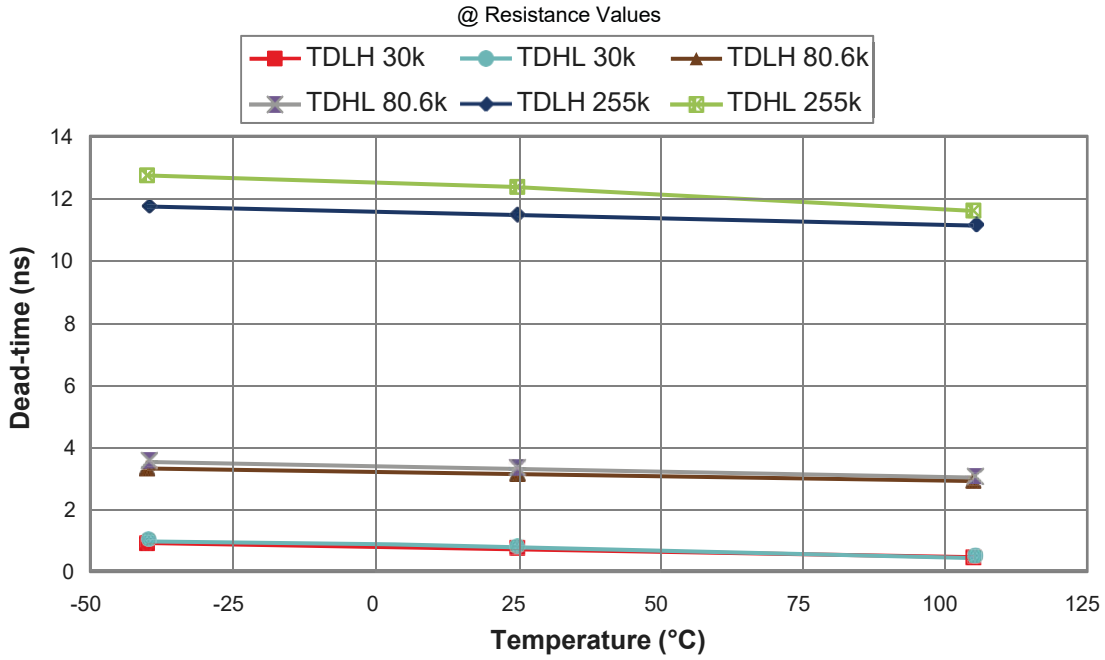


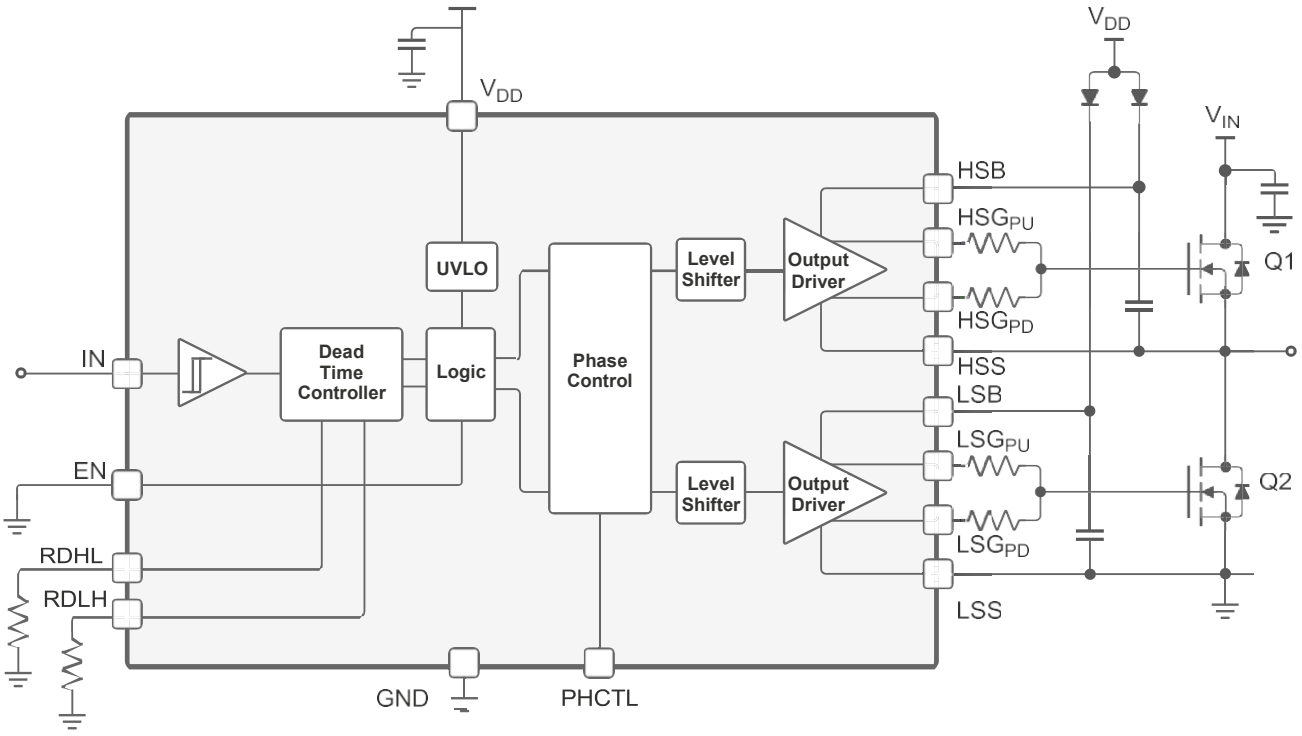
Figure 4 • *Dead-time vs Temperature*



Test Diagram

Figure 5 shows the test circuit used for obtaining measurements. The two bootstrap diodes shown in the schematic are used for symmetry purposes in characterization. In practice, only the HSB diode is required. Removing the LSB diode will result in higher low-side supply voltage since the diode drop is eliminated. As a result, the dead-time resistor can be adjusted to compensate for any changes in propagation delay.

Figure 5 • *Test Circuit for* ***TD99102***



Theory of Operation

General

The TD99102 is intended to drive both the high-side (HS) and the low-side (LS) gates of external power transistors such as eGaN HEMTs and MOSFETs, such as eGaN FETs, for power management applications. The TD99102 favors applications requiring higher switching speeds due to the reduced parasitic properties of the high resistivity insulating substrate inherent with Peregrine's UltraCMOS process.

The driver uses a single-ended pulse width modulation (PWM) input that feeds a dead-time controller, capable of generating a small and accurate dead-time. The dead-time circuit prevents shoot-through current in the output stage. The propagation delay of the dead-time controller must be small to meet the fast switching requirements when driving eGaN FETs. The differential outputs of the dead-time controller are then level-shifted from a low-voltage domain to a high-voltage domain required by the output drivers.

Each of the output drivers includes two separate pull-up and pull-down outputs allowing independent control of the turn-on and turn-off gate loop resistance. The low impedance output of the drivers improves external power FETs switching speed and efficiency, and minimizes the effects of the voltage rise time (dv/dt) transients.

Under-voltage Lockout

An internal under-voltage lockout (UVLO) feature prevents the TD99102 from powering up before input voltage rises above the UVLO threshold of 3.6 V (typ), and 200 mV (typ) of hysteresis is built in to prevent false triggering of the UVLO circuit. The UVLO must be cleared and the EN pin must be released before the part will be enabled.

Dead-time Adjustment

The TD99102 features a dead-time adjustment that allows the user to control the timing of the LS and HS gates to eliminate any large shoot-through currents, which could dramatically reduce the efficiency of the circuit and potentially damage the eGaN FETs. Two external resistors control the timing of outputs in the dead-time controller block. The timing waveforms are illustrated in **Figure 6**.

The dead-time resistors only affect the LS output; the HS output will always equal the duty-cycle of the input. The HS FET gate node will track the duty cycle of the PWM input with a shift in the response, as both rising and falling edges are shifted in the same direction. The LS FET gate node duty cycle can be controlled with the dead-time resistors as each resistor will move the rising and falling edges in opposite directions. RDLH will change the dead-time from low-side gate (LSG) falling to high-side gate (HSG) rising and RDHL will change the dead-time from HSG falling to LSG rising. **Figure 7** shows the resulting dead-time versus the external resistor values with both HS and LS bias diode/capacitors installed as indicated in **Figure 2**. The LS bias diode and also the capacitor are included for symmetry only and they are not required for the part to function. Removing the LS bias diode will increase the LSG voltage by approximately 0.3 V, resulting in a wider separation of the t_{DHL} and t_{DLH} curves in **Figure 7**.

Phase Control

Pin 10 (PHCTL) controls the polarity of the gate driver outputs. When PHCTL is low, the HSG will be in phase with the input signal. When PHCTL is high, the LSG will be in phase with the input signal. The PHCTL pin includes an internal pull-down resistor and can be left floating.

Figure 6 and **Figure 7** provide the dead-time description for the TD99102.

Figure 6 • *Dead-time Description* ***TD99102***

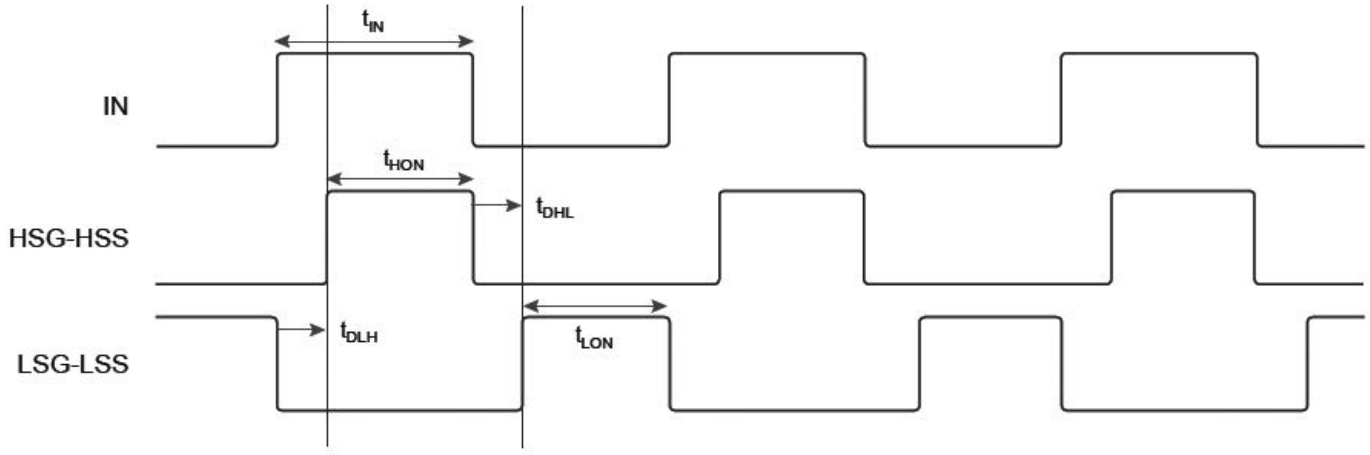


Figure 7 • *Dead-time between HSG and LSG (ns)*

Application Circuit

Figure 8 shows a typical application diagram of the TD99102 and its external components in a half-bridge configuration(*). The TD99102 is designed to provide a LS gate driver, referenced to ground, and a floating HS gate driver referenced to the switch node (HSS). A common technique to generate the floating HS gate drive uses a bootstrap diode in conjunction with a decoupling capacitor. However, if the LS device conducts currents through its body diode during the dead-time period, an overvoltage condition across the bootstrap capacitor can result.

A more elegant approach replaces the HS bootstrap diode with a GaN transistor (Q3). The GaN HEMT is used as a synchronous bootstrap to prevent overvoltage of the HS device. This is accomplished by synchronously switching Q3 using the LSG signal so that Q3 turns on and charges the bootstrap capacitor when LSG is high, but turns off as soon as LSG turns low so that no inadvertent bootstrap overcharging occurs during the dead-time periods.

The external gate resistors are required to de-Q the inductance in the gate loop and dampen any ringing on the GaN transistor gates and the SW node.

Dead-time resistors RDHL and RDLH can be adjusted to compensate for any changes in propagation delay.

Note: * For applications greater than 30V in a half-bridge configuration, the TD99102 can be sensitive to high dv/dt conditions on HSS.

Figure 8 • *Applications Diagram for* ***TD99102***

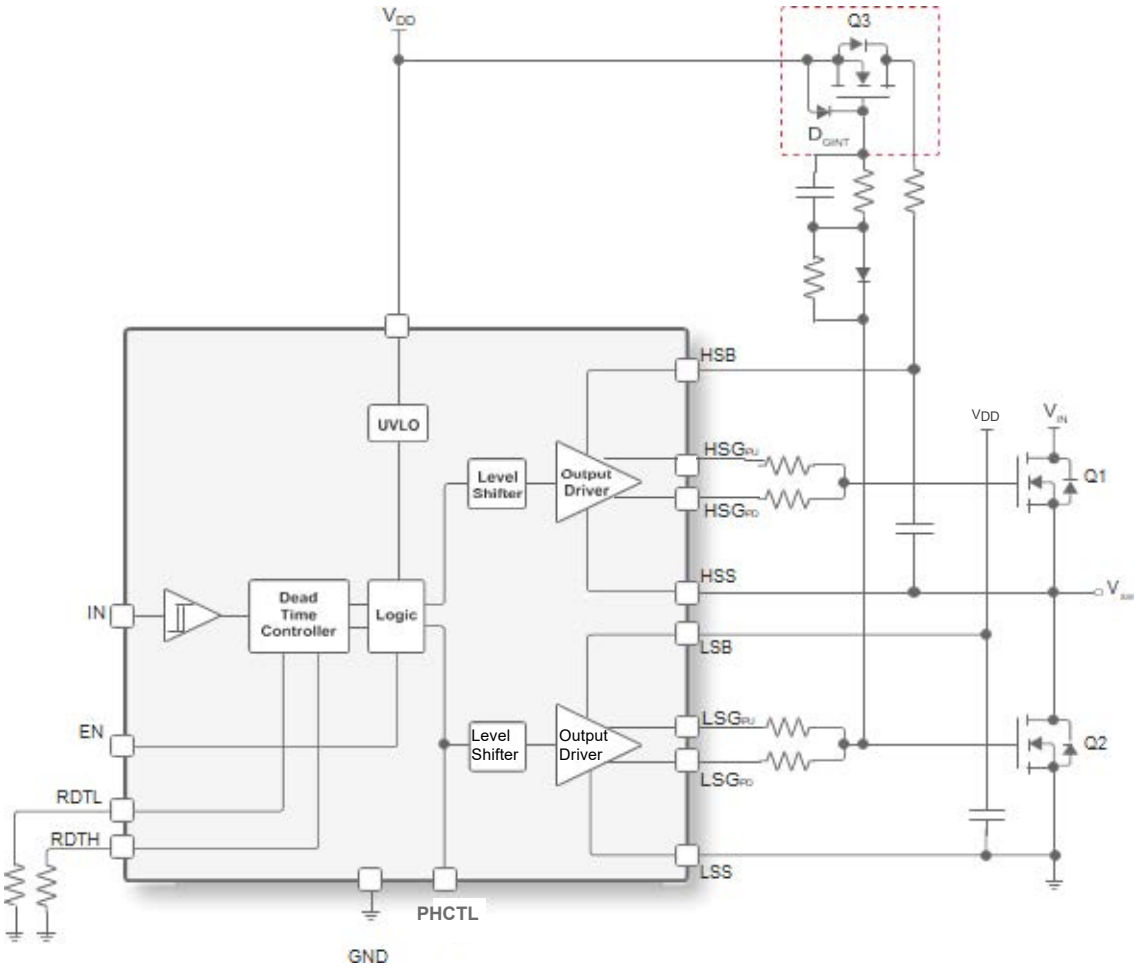
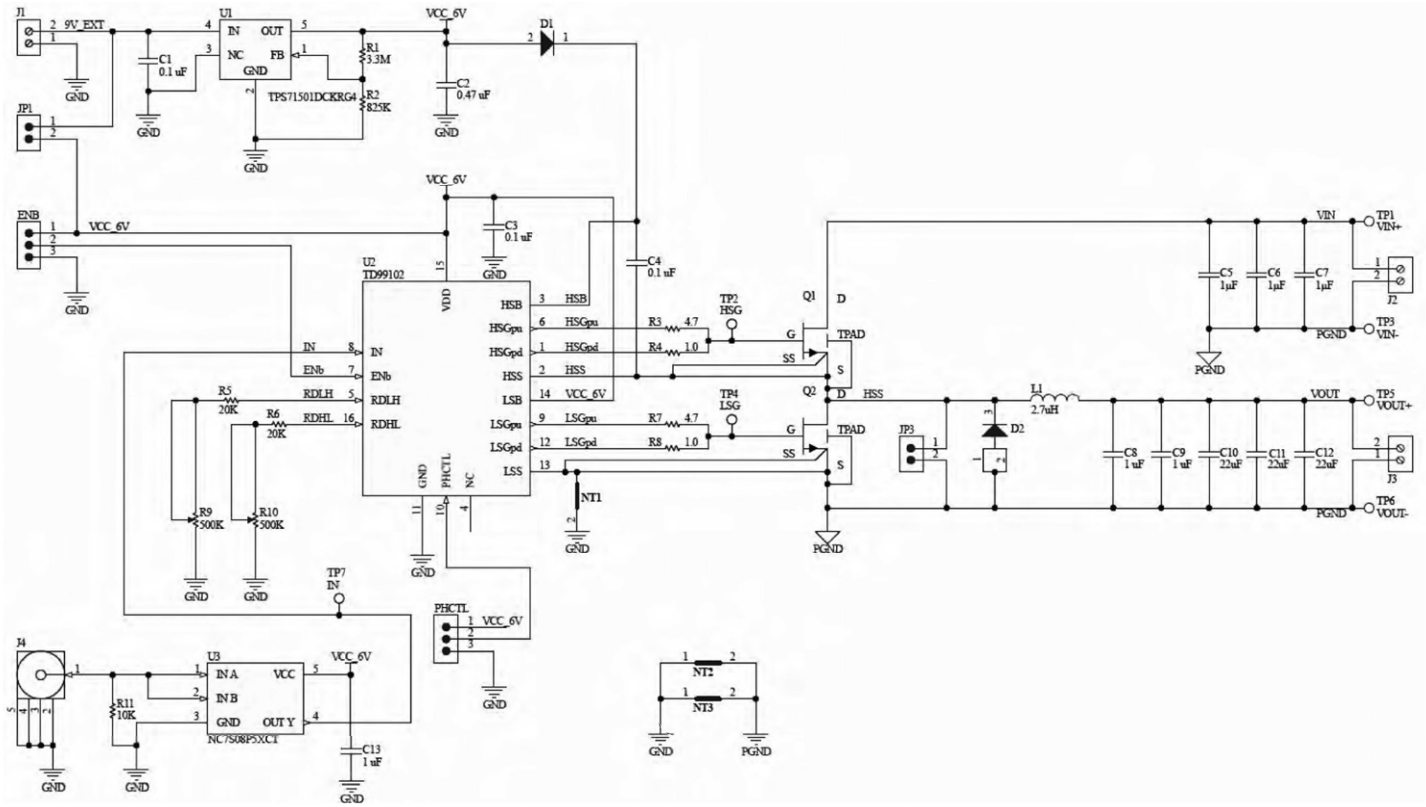


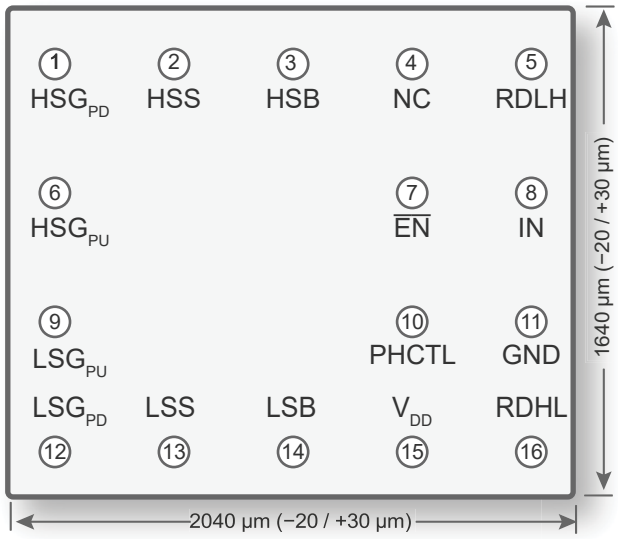
Figure 9 • *Applications Diagram for* ***TD99102***

Suggested Reference Design with TDG100E90 100V E-mode GaN transistor



Pin Configuration

Figure 10 • *Pin Configuration (Bumps Up)*



Notes:

1) Drawings are not drawn to scale.
2) Singulated die size shown, bump side up.
3) NC = No Connect / Must remain open.
4) Bump compostion = SAC351
   a) Reflow / See link: **Application Note 66**

Table 5 • *Pin Descriptions for TD99102*

Pin No.	Pin Name	Description
1	HSG_{PD}	High-side gate drive pull-down
2	HSS	High-side source
3	HSB	High-side bias
4	NC	No connection (ground or float)
5	RDLH	Dead-time control resistor sets LSG falling to HSG rising delay (external resistor to GND)
6	HSG_{PU}	High-side gate drive pull-up
7(*)	$\overline{EN}$	Enable active low, tri-state outputs when high
8(*)	IN	Control input
9	LSG_{PU}	Low-side gate drive pull-up
10(*)	PHCTL	Controls the polarity of the gate driver outputs
11	GND	Ground
12	LSG_{PD}	Low-side gate drive pull-down
13	LSS	Low-side source
14	LSB	Low-side bias
15	V_{DD}	+5V supply voltage
16	RDHL	Dead-time control resistor sets HSG falling to LSG rising delay (external resistor to ground)

Note: * Internal 100k pull down resistor

Die Mechanical Specifications

This section provides the die mechanical specifications for the TD99102.

Table 6 • *Die Mechanical Specifications for* ***TD99102***

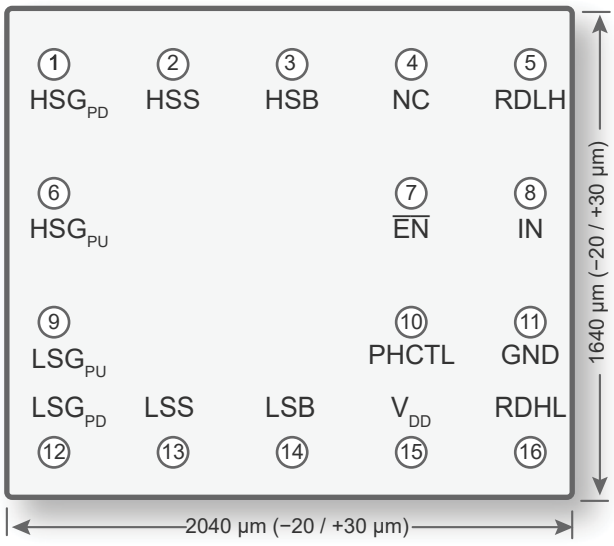
Parameter	Min	Typ	Max	Unit	Test Condition
Die size, singulated (x,y)		2040 × 1640		µm	Including sapphire, max tolerance = –20/+30
Bump pitch		400		µm	
Bump height		85		µm	
Bump diameter		110		µm	max tolerance = ±17

Table 7 • *Die Pad Coordinates for* ***TD99102***[*]

Pin #	Pin Name	Pin Center (µm)	
		X	Y
1	HSG_{PD}	–800	600
2	HSS	–400	600
3	HSB	0	600
4	NC	400	600
5	RDLH	800	600
6	HSG_{PU}	–800	200
7	$\overline{EN}$	400	200
8	IN	800	200
9	LSG_{PU}	–800	–200
10	PHCTL	400	–200
11	GND	800	–200
12	LSG_{PD}	–800	–600
13	LSS	–400	–600
14	LSB	0	–600
15	V_{DD}	400	–600
16	RDHL	800	–600

Note: * All pad locations originate from the die center and refer to the center of the pad.

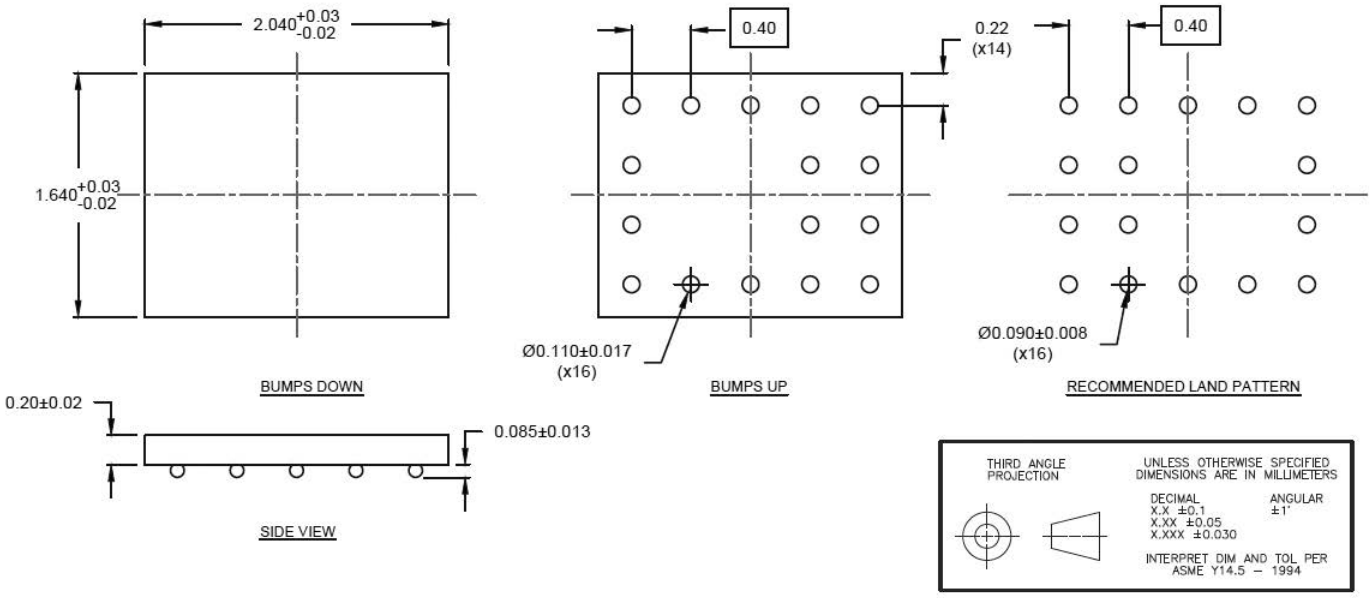
Figure 11 • *Die Pad Layout for* ***TD99102***[(1)(2)]



Notes:

1) Drawings are not drawn to scale.
2) Singulated die size shown, bump side up.
3) NC = No Connect / Must remain open.
4) Bump compostion = SAC351
   a) Reflow / See link: **Application Note 66**

Figure 12 • *Recommended Land Pattern for* ***TD99102***



TD99102

Ordering Information

Table 8 lists the available ordering code for the TD99102

Table 8 • *Order Codes for* ***TD99102***

Order Codes	Description	Packaging	Shipping Method
TD99102-98	99102 EM Die*	Waffle Pack	Waffle Pack
TD99102-99	99102 Flight Die	Waffle Pack	Waffle Pack
TD99102-00	99102 EVK	Box	Box

Note: *The -98 devices are EM (engineering model) prototype units intended for use as initial evaluation units for customers. They provide the same functionality and footprint as Flight Die and are intended for engineering evaluation only. These units are not suitable for qualification, production, radiation testing or flight use.

Document Revision History:

Document No.	Description	Date
TD99102_02_2022 Rev 1	Initial Release	02/11/2022
TD99102_06_02_2022 Rev 2	1) Remove max limits for Dead-time: HSG going low to LSG going high and LSG going low to HSG going high. 2) Remove max limits for Table 3 dc Characteristics except leave Total quiescent current VDD= 5 V and VDD = 6 V. 3) Note added to Table 3. 4) -98 EM die orderable added + EM Note.	06/02/2022
TD99102_05_02_2024 Rev 3	1) Added EVK to Ordering Information Table 8	05/02/2024

Document Categories and Definitions

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Teledyne e2v HiRel Electronics reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Teledyne e2v HiRel Electronics decides to change the specifications, Teledyne e2v HiRel Electronics will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

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