TDLNA0430SEP: 0.03 – 3.0 GHz GaAs Ultra Low Noise Amplifier

1.0 Features

- Small signal gain @ 1800 MHz: 21.5 dB
- NF @ 1800 MHz: 0.35 dB
- OP1dB @ 1800 MHz: 12 dBm
- OIP3dB @ 1800 MHz: 30 dBm
- 5 V Typical operating voltage
- Operating frequency: 0.03 to 3.0 GHz

Top Side Bottom Side

Figure 1.1 Device Image
8 Pin 2×2×0.75 mm QFN Package)

RoHS/REACH/Halogen Free Compliance

2.0 Applications

- 4G/5G Infrastructure Radios
- Small Cells and Cellular Repeaters
- Phased Array Radar
- SDARS

3.0 Description

The TDLNA0430SEP is a broadband, ultra-low Noise Amplifier (LNA) providing high gain and linearity. With a simple input and output match, this LNA can be tuned for different frequency bands targeting LTE (small cells and infrastructure) and any other applications requiring low noise, high gain, and linearity. For >3 GHz frequency band, TDLNA2050SEP can be considered.
The TDLNA0430SEP is packaged in a compact, low-cost Dual Flat No Lead (DFN) 2 x 2 x 0.75 mm, 8-pin, plastic package.

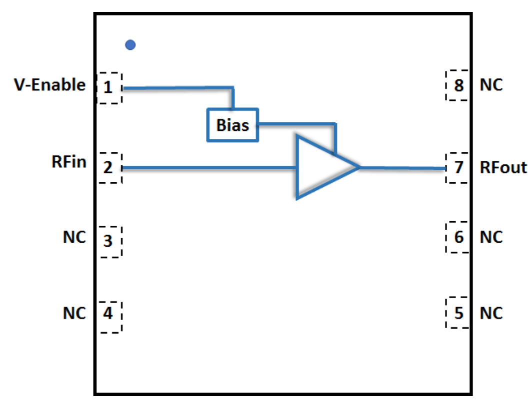


Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Base Part Number	Package Type	Orderable Part Number
TDLNA0430S	8 Pin 2×2×0.75 mm DFN	TDLNA0430SEP
Tuned Evaluation Board, 1800 - 2100 MHz		TDLNA0430-EVB-A
Tuned Evaluation Board, 2500 - 2700 MHz		TDLNA0430-EVB-B
Tuned Evaluation Board, 30 - 1000 MHz		TDLNA0430-EVB-C
Tuned Evaluation Board, 30-2600 MHz [3.3 V 30 mA]		TDLNA0430-EVB-D1
Tuned Evaluation Board, 30-2600 MHz [5 V 55 mA]		TDLNA0430-EVB-D2
Tuned Evaluation Board, 1000-2000 MHz		TDLNA0430-EVB-E

5.0 Pin Description

Table 5.1 Pin Definition

Pin Number	Pin Name	Description
3-6, 8	NC	No internal connection, can be connected to ground
1	V_{enable}	V_{enable} along with series resistor, sets the Idq. V_{enable} <0.2 V disables the device
2	RF_{IN}	RF Input. DC blocking cap required
7	RF_{OUT}/V_{dd}	RF Output. Vdd supplied through an external choke inductor
Package Base	Paddle/Slug	DC and RF Ground. Also provides thermal relief. Multiple vias are recommended

Note: [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heatsinking required.

6.0 Absolute Maximum Rating

Table 6.1 Absolute Maximum Rating @T_A = +25 °C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Supply voltage, V_{enable}	V_{dd}	+6	V
Drain current	I_{DQ}	70	mA
RF input power CW	RF_{IN}	23	dBm
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-55 to +125	°C
Maximum Junction Temperature	T_J	170	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{θJC}$	15.0	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Recommended DC Operating Conditions

Table 7.1 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltage	V_{DD}		+5.0		V
Venable Voltage	V_{enable}		+5.0		V
Drain Bias Current	$I_{DQ,}$ Set by external resistor	45	60		mA
Venable Bias Current	I_{bias}		3.0		mA
Operating Temperature Range		-55	+25	+125	°C

8.0 Switching Time

Table 8.1 Switching time.

Parameter	Test Condition	Typical	Unit
Switching Rise Time /1	10/90% of the RF value	300	nsec
Switching Fall Time /1	10/90% of the RF value	350	nsec

9.0 RF Electrical Specifications

Table 9.1 EVB A 1800-2100 MHz

Venable = 5 V, Idd = 60 mA, Vdd = 5 V, @T_A = +25 °C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across band	13	20-22	30	dB
Noise Figure /1	Across band		0.35-0.45		dB
EVB Noise Figure /1	Across band		0.4-0.5		dB
Input Return Loss	Across band	-10	17-27		dB
Output Return Loss	Across band	-5	- 8.5 to -10		dB
OP1dB	Across band	12	18-19.5		dBm
OIP3 /1	Across the band, 0dBm per tone, Tone Spacing 1 MHz		35-37.5		dBm

All parametric data displayed in Tables 7.1 to 9.1 designated with /1 footnote are not tested in Production.

Table 9.2 EVB B 2500-2700 MHz

Venable = 5 V, Idd = 60 mA, Vdd = 5 V , @T_A = +25 °C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band		19.2-18.5		dB
Noise Figure	Across Band		0.45		dB
EVB Noise Figure	Across Band		0.5		dB
Input Return Loss	Across Band		27-33		dB
Output Return Loss	Across Band		-9		dB
OP1dB	Across Band		18.4-19.6		dBm
OIP3	Across Band, 0dBm per tone, Tone Spacing 1 MHz		41-43		dBm

All parametric data displayed in Tables 9.2 to 9.6 are not tested in Production.

Table 9.3 EVB C 30-1000 MHz

Venable = 3.3 V, Idd = 30 mA, Vdd = 3.3 V, @T_A = +25 °C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across band		25.6-21.3		dB
Noise Figure	Across band		0.5-0.3		dB
EVB Noise Figure /	Across band		0.6-0.3		dB
Input Return Loss	Across band		12.5-26		dB
Output Return Loss	Across band		-7.4 to -19.3		dB
OP1dB	Across band		-14.4 to -15.2		dBm
OIP3	Across the band, 0dBm per tone, Tone Spacing 1 MHz		27.5-29.3		dBm

Table 9.4 EVB D1 30-2600 MHz

Venable = 3.3 V, Idd = 30 mA, Vdd = 3.3 V, @T_A = +25 °C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across band		20.3-13.6		dB
Noise Figure	Across band		0.6-0.4		dB
EVB Noise Figure	Across band		0.7-0.4		dB
Input Return Loss	Across band		8.3-16		dB
Output Return Loss	Across band		-7.4 to -19.3		dB
OP1dB	Across band		12.1-14.7		dBm
OIP3	Across the band, 0dBm per tone, Tone Spacing 1 MHz		22.6-29		dBm

Table 9.5 EVB D2 30-2600 MHz

Venable = 5 V, Idd = 55 mA, Vdd = 5 V, @T_A = +25 °C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across band		21.9-13.5		dB
Noise Figure	Across band		0.7-0.5		dB
EVB Noise Figure	Across band		0.8-0.5		dB
Input Return Loss	Across band		8.9-23.5		dB
Output Return Loss	Across band		-6.4 to -19.6		dB
OP1dB	Across band		13.8-17.8		dBm
OIP3	Across the band, 0dBm per tone, Tone Spacing 1 MHz		27.2-33		dBm

Table 9.6 EVB E 1000-2000 MHz

Venable = 3.3 V, Idd = 50 mA, Vdd = 3.3 V, @T_A = +25 °C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across band		23.6-18.5		dB
Noise Figure	Across band		0.45-0.4		dB
EVB Noise Figure	Across band		0.5-0.4		dB
Input Return Loss	Across band		12.5-26		dB
Output Return Loss	Across band		-5.1 to -21.5		dB
OP1dB	Across band		5.4-6.7		dBm
OIP3	Across the band, 0dBm/ tone, Tone Spacing 1 MHz		27.5-29.3		dBm

10.0 Evaluation Board Details

10.1 EVB A 1.8-2.1 GHz

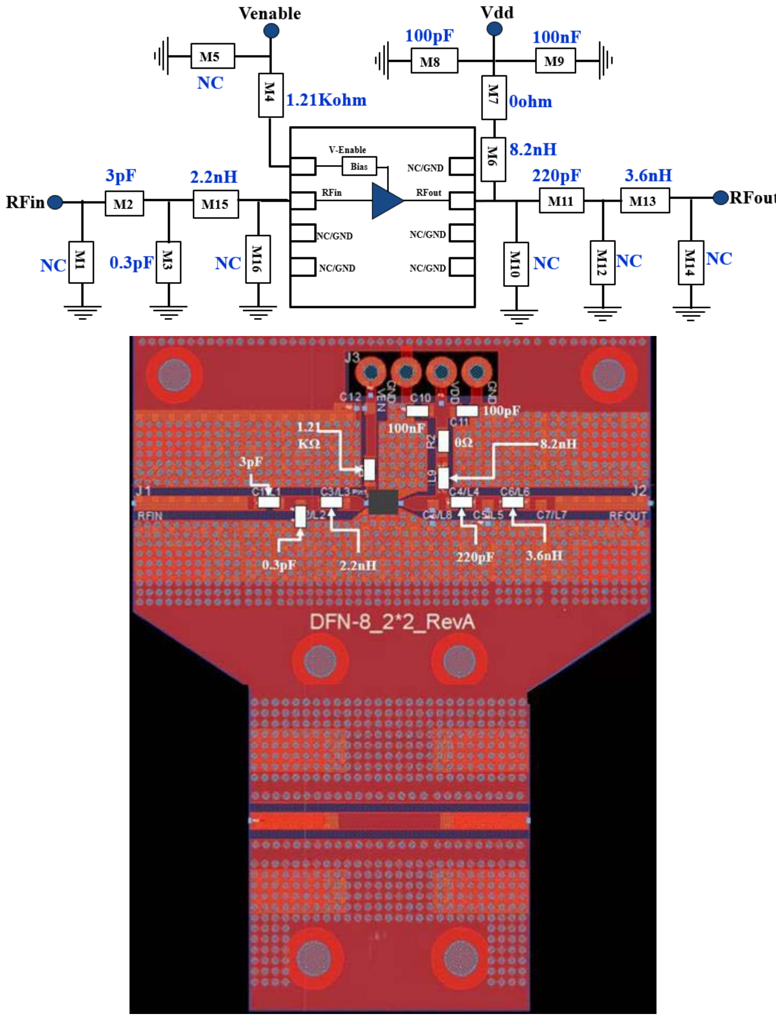
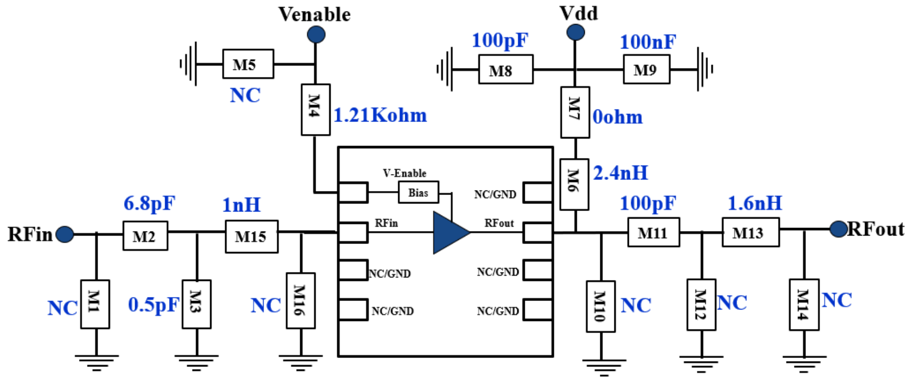


Figure 10.1 Schematic and EVB layout of the 1800-2100 MHz EVB-A

Table 10.1 BOM of the 1800-2100 MHz EVB A

Component ID	Value	Manufacturer	Recommended Part Number
M2	3.0 pF	Murata	GJM1555C1H3R0BB01
M3	0.3 pF	Murata	GJM1555C1HR30BB01
M15	2.2 nH	Coil craft /Wurth Elektronik	0402HP-2N2XJE /744765022A
M4	1.21 kΩ	Panasonic	ERJ-2RKF1211X
M8	100 pF	AVX	04025A101JAT4A
M9	100 nF	TDK	C1005X7R1H104K050BE
M7	0 Ω	Panasonic	ERJ-2GE0R00X
M6	8.2 nH	Coil craft /Wurth Elektronik	0402HP-8N2XGE /744765082GA
M11	220 pF	Kemet	C0402C221K5GACAUTO
M13	3.6 nH	Coil Craft /Wurth Elektronik	0402HP-3N6XGE /744765036A
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

10.2 EVB B 2.5-2.7 GHz



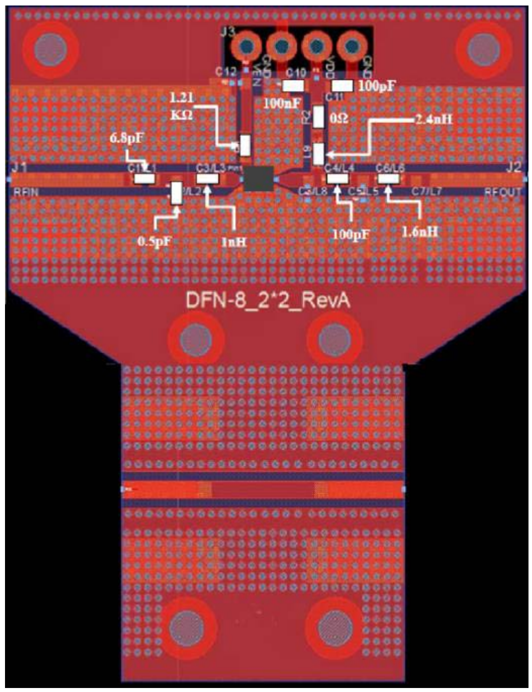


Figure 10.2 Schematic and EVB layout of the 2500-2700 MHz EVB-B

Table 10.2 BOM of the 2500-2700 MHz EVB B

Component ID	Value	Manufacturer	Recommended Part Number
M2	6.8 pF	Murata	GJM1555C1H6R8BB01
M3	0.5 pF	Murata	GJM1555C1HR50BB01
M15	1 nH	Coil craft	0402HP-1N0XJE
M4	1.21 kΩ	Panasonic	ERJ-2RKF1211X
M8	100 pF	AVX	04025A101JAT4A
M9	100 nF	TDK	C1005X7R1H104K050BE
M7	0 Ω	Panasonic	ERJ-2GE0R00X
M6	2.4 nH	Coil craft	0402HP-2N4XGE
M11	100 pF	AVX	04025A101JAT4A
M13	1.6 nH	Coil craft	0603HC-1N6XGLW
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

10.3 EVB C 30-1000 MHz

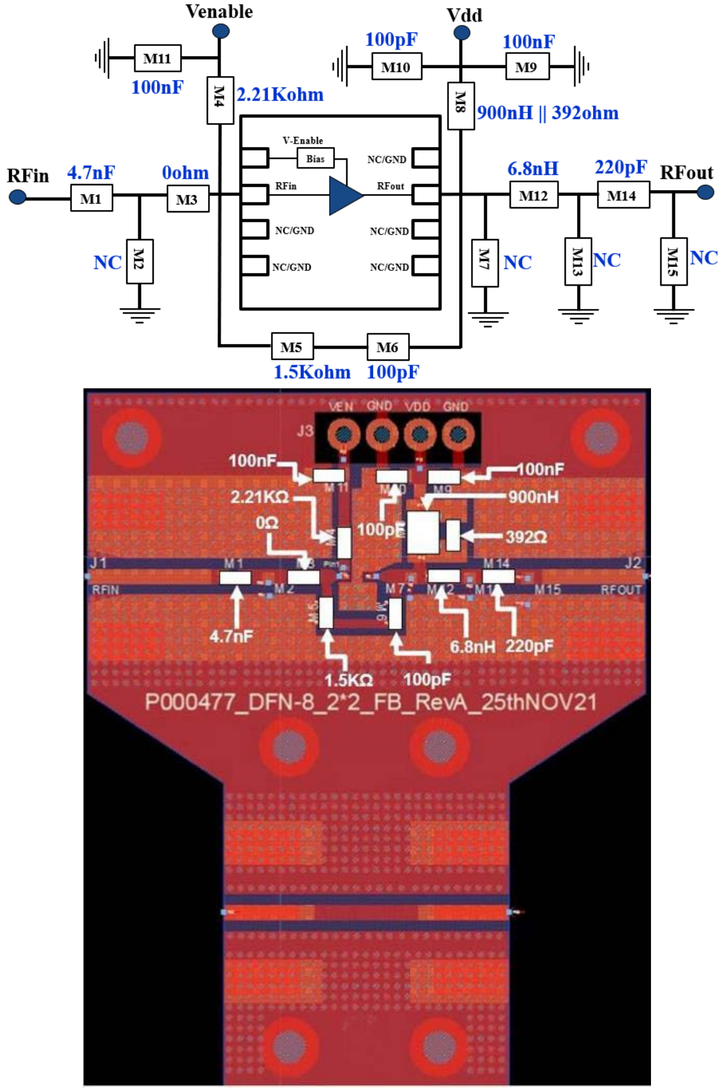


Figure 10.3 Schematic and EVB layout of the 30-1000 MHz EVB-C

Table 10.3 BOM of the 30-1000 MHz EVB C

Component ID	Value	Manufacturer	Recommended Part Number
M1	4.7 nF, 50 V	Murata	GRM1885C1H472JA01D
M3	0 Ω	Panasonic	ERJ-2GE0R00X
M4	2.21 kΩ	Panasonic	ERJ-2RKF2211X
M5	1.5 kΩ	Panasonic	ERJ-2RKF1501X
M6, M10	100 pF	AVX	04025A101JAT4A
M8	900 nH	Coil craft	1008AF-901XJLC
M8	392 Ω	Panasonic	ERJ-UP3F3920V
M9, M11	100 nF	TDK	C1005X7R1H104K050BE
M12	6.8 nH	Coil craft	0402HP-6N8XJRW
M14	220 pF	Kemet	C0402C221K5GACAUTO
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

10.4 EVB D1 30-2600 MHz

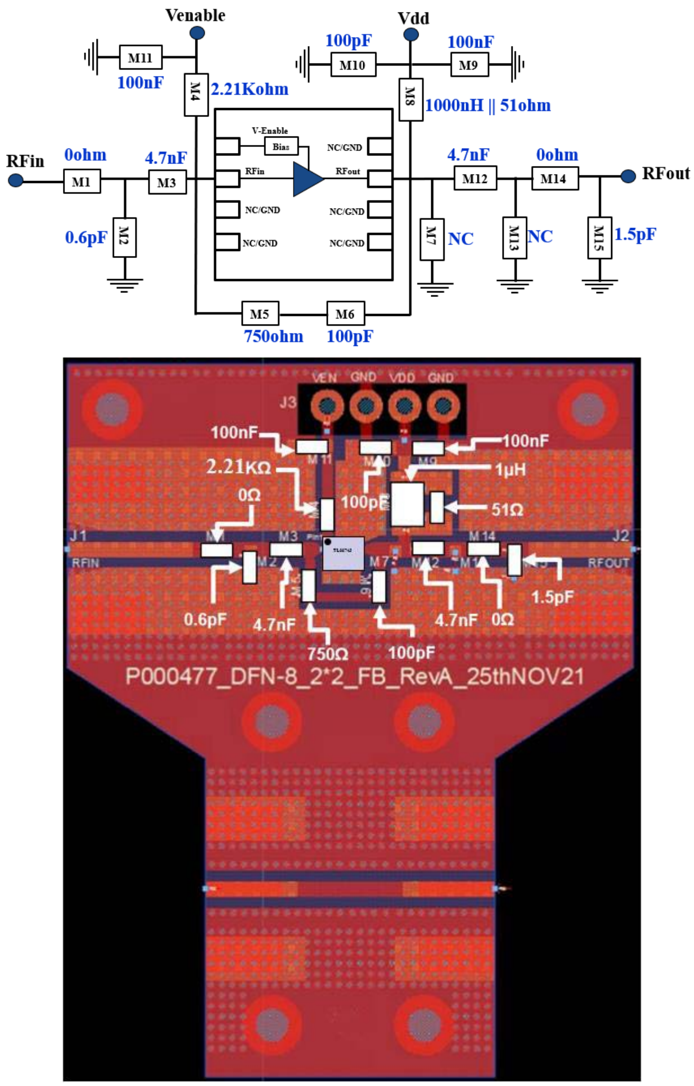


Figure 10.4 Schematic and EVB layout of the 30-2600 MHz EVB-D1

Table 10.4 BOM of the 30-2600 MHz EVB D1

Component ID	Value	Manufacturer	Recommended Part Number
M1, M14	0 Ω	Panasonic	ERJ-2GE0R00X
M2	0.6 pF	Murata	GJM1555C1HR60BB01D
M3, M12	4.7 nF, 50 V	Murata	GRM1885C1H472JA01D
M4	2.21 kΩ	Panasonic	ERJ-2RKF2211X
M5	750 Ω	KOA Speer	RK73H1ERTTP7500F
M6, M10	100 pF	AVX	04025A101JAT4A
M8	1 µH	Coil craft	PFL2512-102MEC
M8	51 Ω	R0HM Semiconductor	ESR03EZPJ510
M9, M11	100 nF	TDK	C1005X7R1H104K050BE
M15	1.5 pF	Murata	GJM1555C1H1R5BB01J
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

10.5 EVB D2 30-2600 MHz

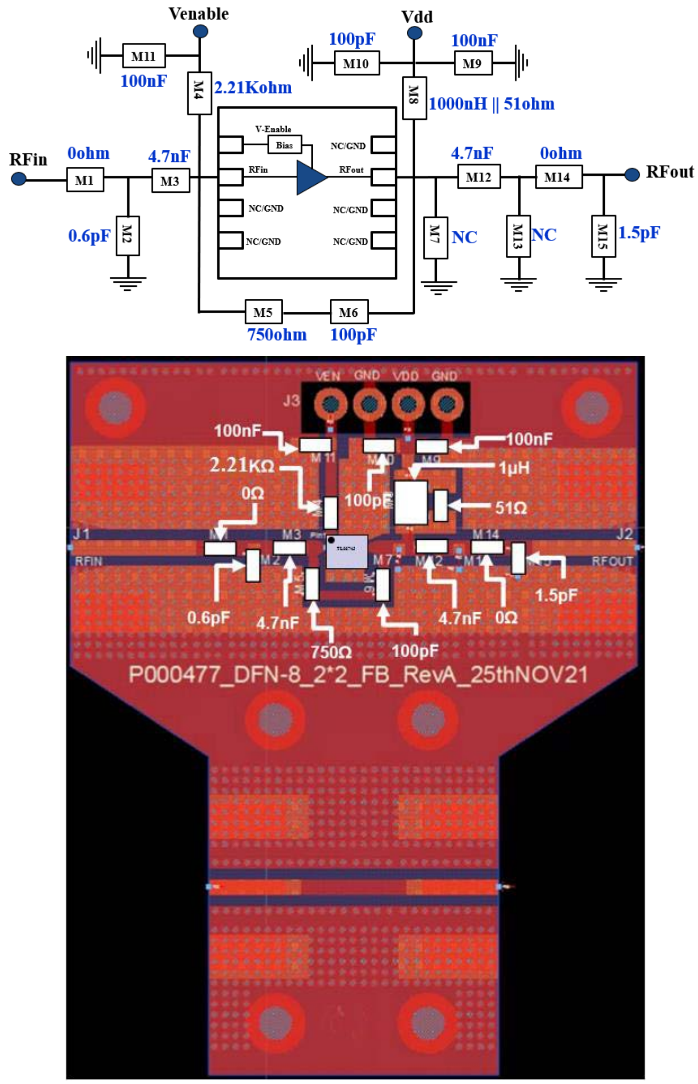


Figure 10.5 Schematic and EVB layout of the 30-2600 MHz EVB-D2

Table 10.5 BOM of the 30-2600 MHz EVB D2

Component ID	Value	Manufacturer	Recommended Part Number
M1, M14	0 Ω	Panasonic	ERJ-2GE0R00X
M2	0.6 pF	Murata	GJM1555C1HR60BB01D
M3, M12	4.7 nF, 50 V	Murata	GRM1885C1H472JA01D
M4	2.21 kΩ	Panasonic	ERJ-2RKF2211X
M5	750 Ω	KOA Speer	RK73H1ERTTP7500F
M6, M10	100 pF	AVX	04025A101JAT4A
M8	1 µH	Coil craft	PFL2512-102MEC
M8	51 Ω	R0HM Semiconductor	ESR03EZPJ510
M9, M11	100 nF	TDK	C1005X7R1H104K050BE
M15	1.5 pF	Murata	GJM1555C1H1R5BB01J
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

10.6 EVB E 1000-2000 MHz

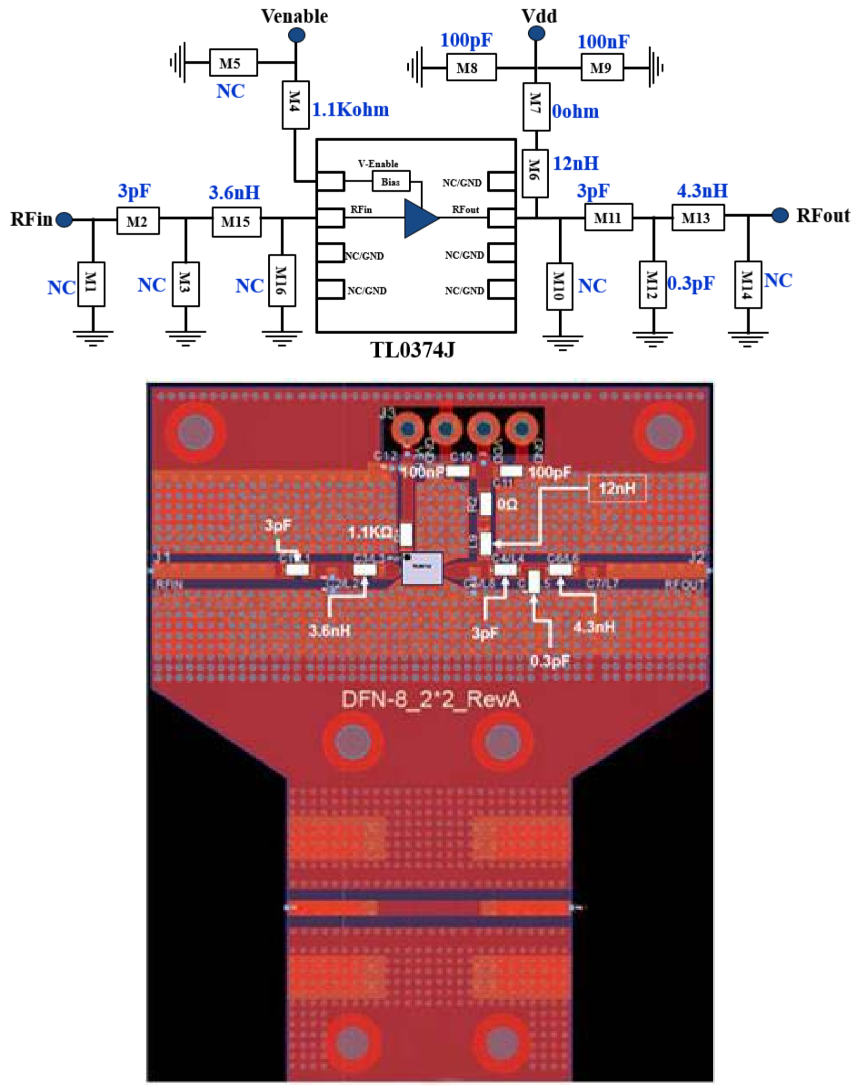


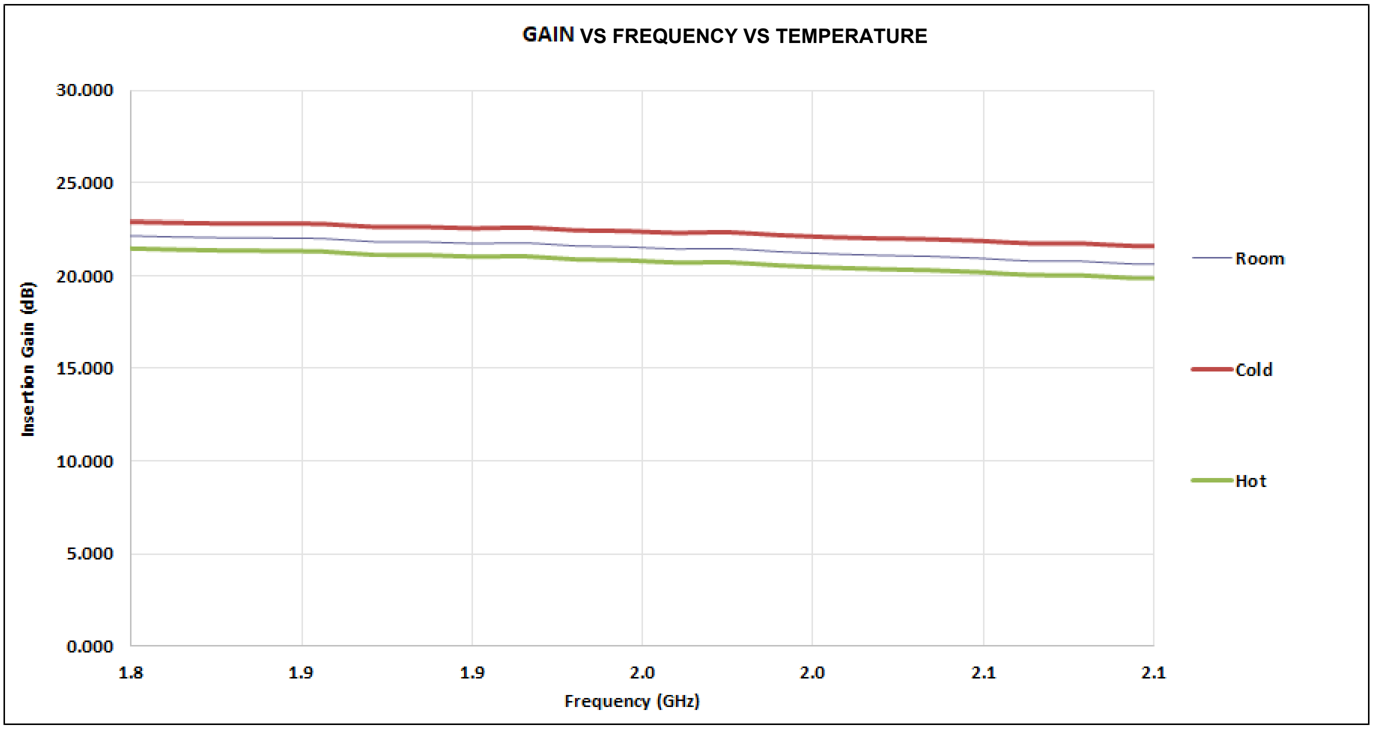
Figure 10.6 Schematic and EVB layout of the 1000-2000 MHz EVB-E

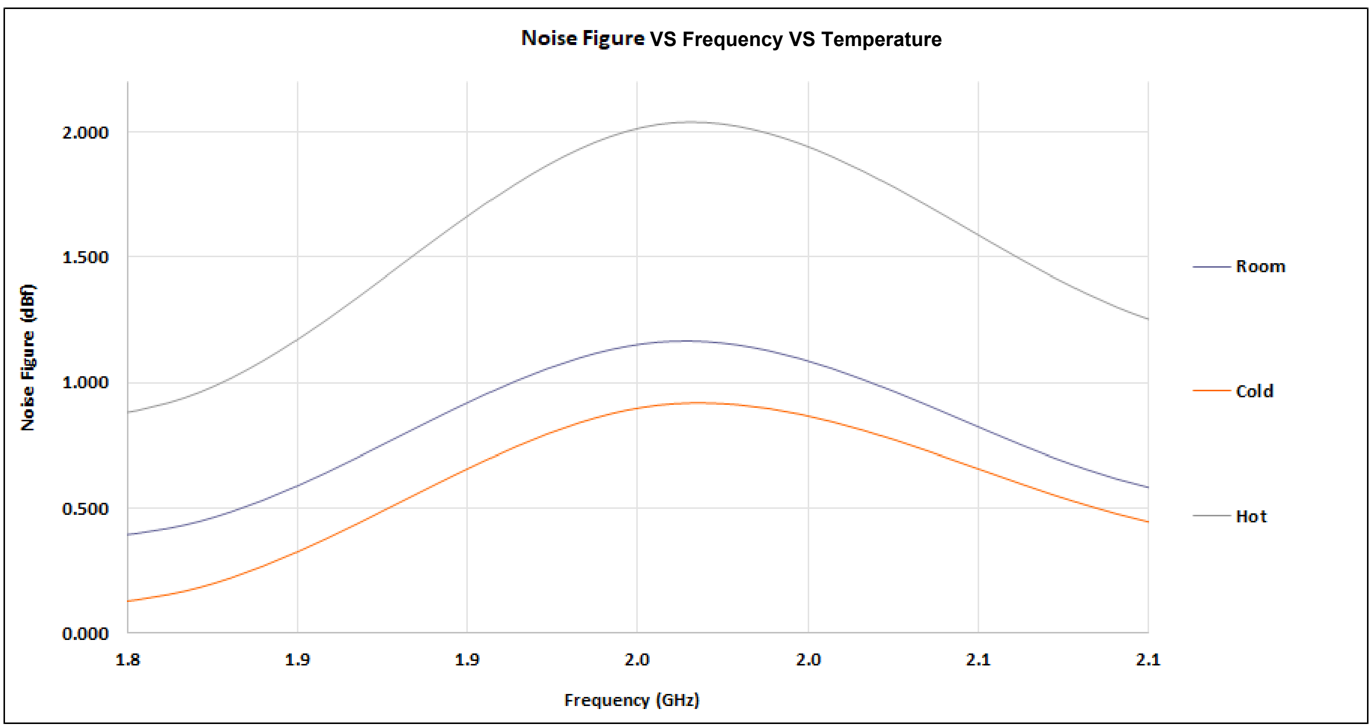
Table 10.6 BOM of the 1000-2000 MHz EVB E

Component ID	Value	Manufacturer	Recommended Part Number
M2, M11	3.0 pF	Murata	GJM1555C1H3R0BB01
M12	0.3 pF	Murata	GJM1555C1HR30BB01
M8	100 pF	AVX	04025A101JAT4A
M9	100 nF	TDK	C1005X7R1H104K050BE
M7	0 Ω	Panasonic	ERJ-2GE0R00X
M6	12 nH	Coil craft	0402HP-12NXE
M15	3.6 nH	Coil craft/Wurth Electronics	0402HP-3N6XGE/744916036
M14	1.1 kΩ	Panasonic	ERJ-2RKF1101X
M13	4.3 nH	Coil craft	0402HP-4N3XGE
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

11.0 Typical Characteristics

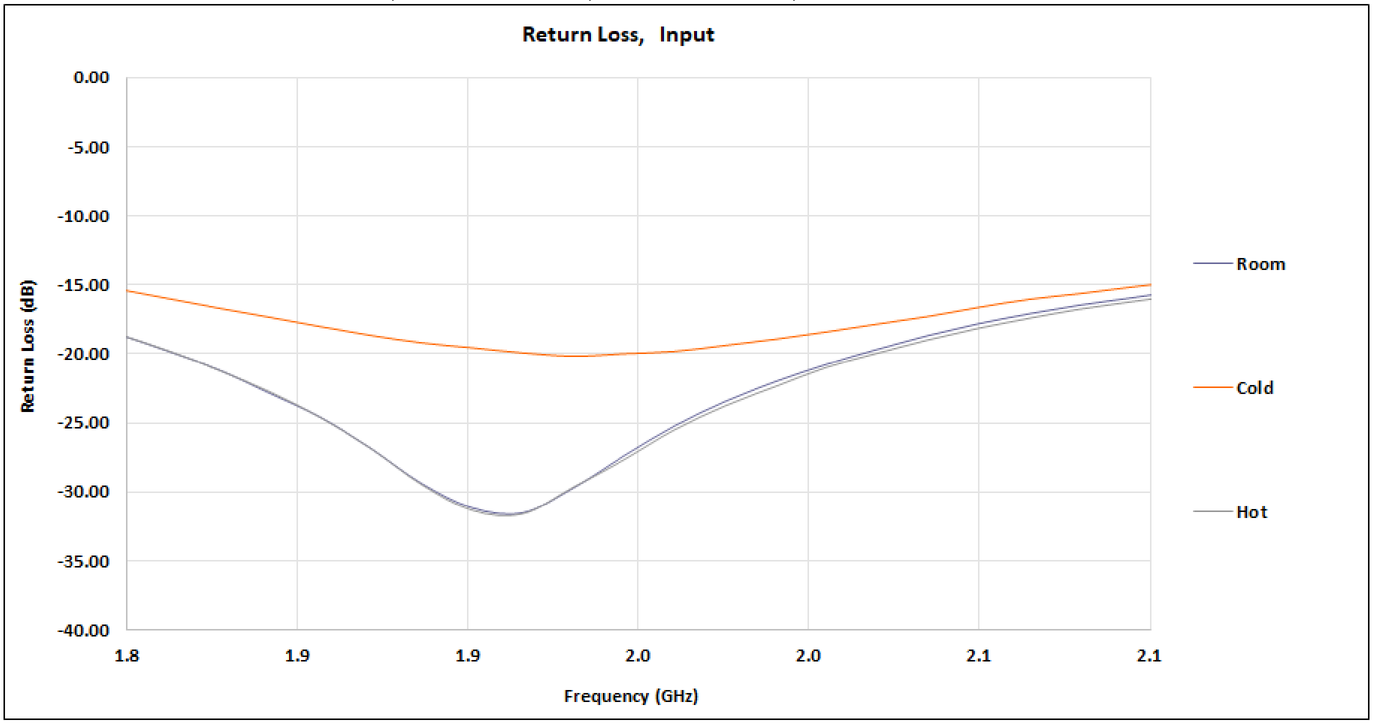
Test Conditions: Vdd = 5 V, Cold = -55 ºC, Room = 25 ºC, Hot = 125 ºC

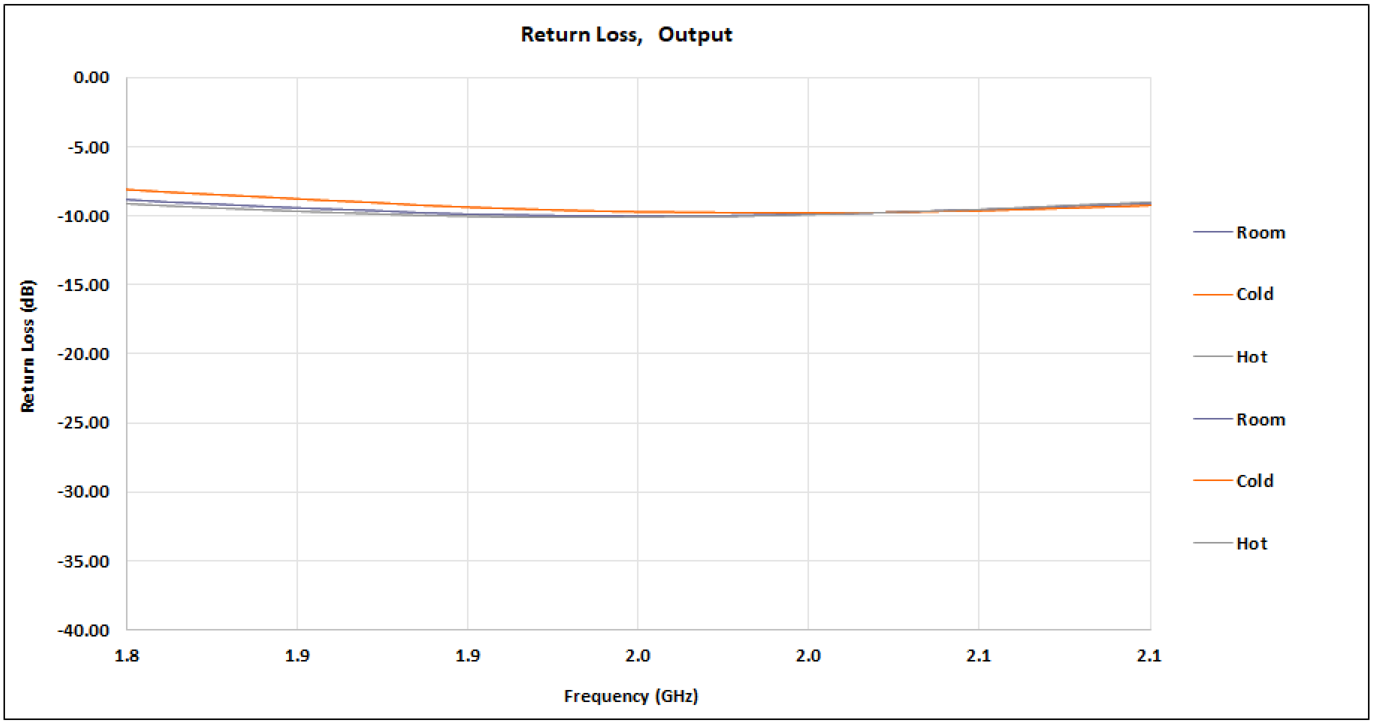




11.0 Typical Characteristics (continued)

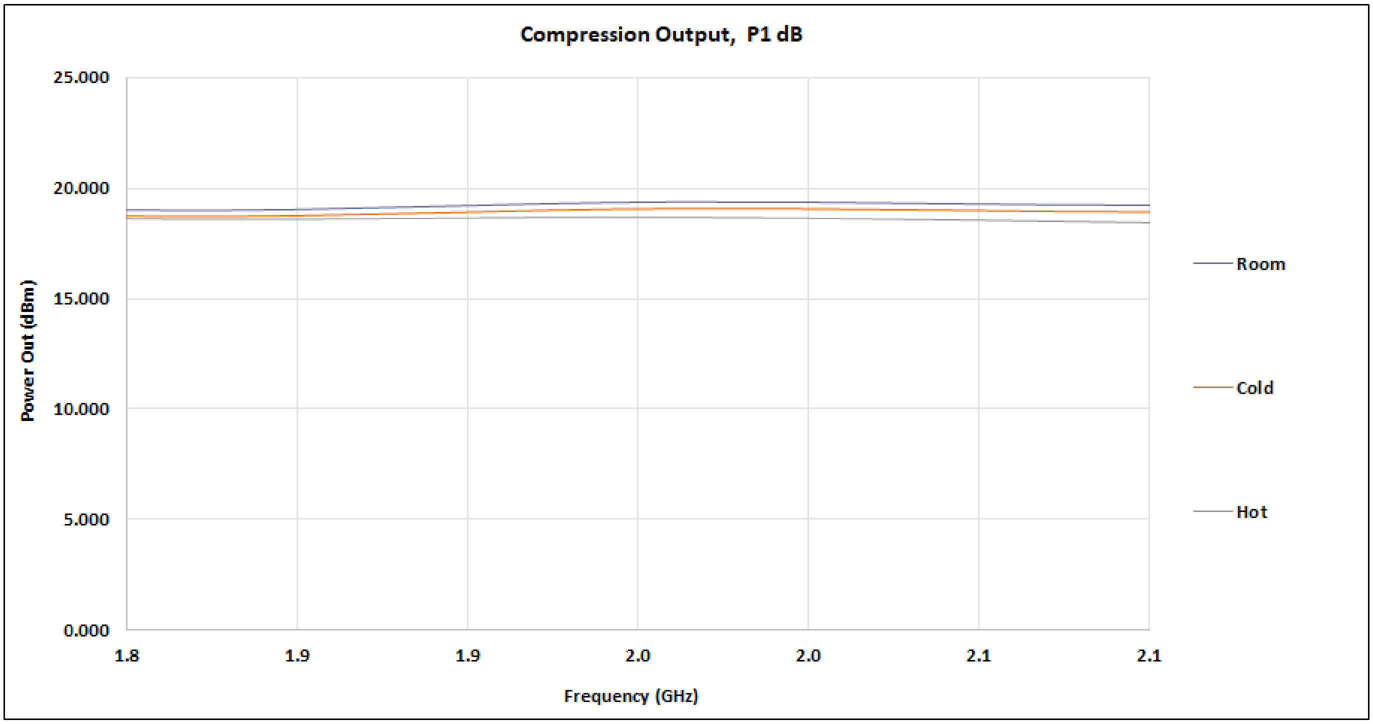
Test Conditions: Vdd = 5 V, Cold = -55 ºC, Room = 25 ºC, Hot = 125 ºC

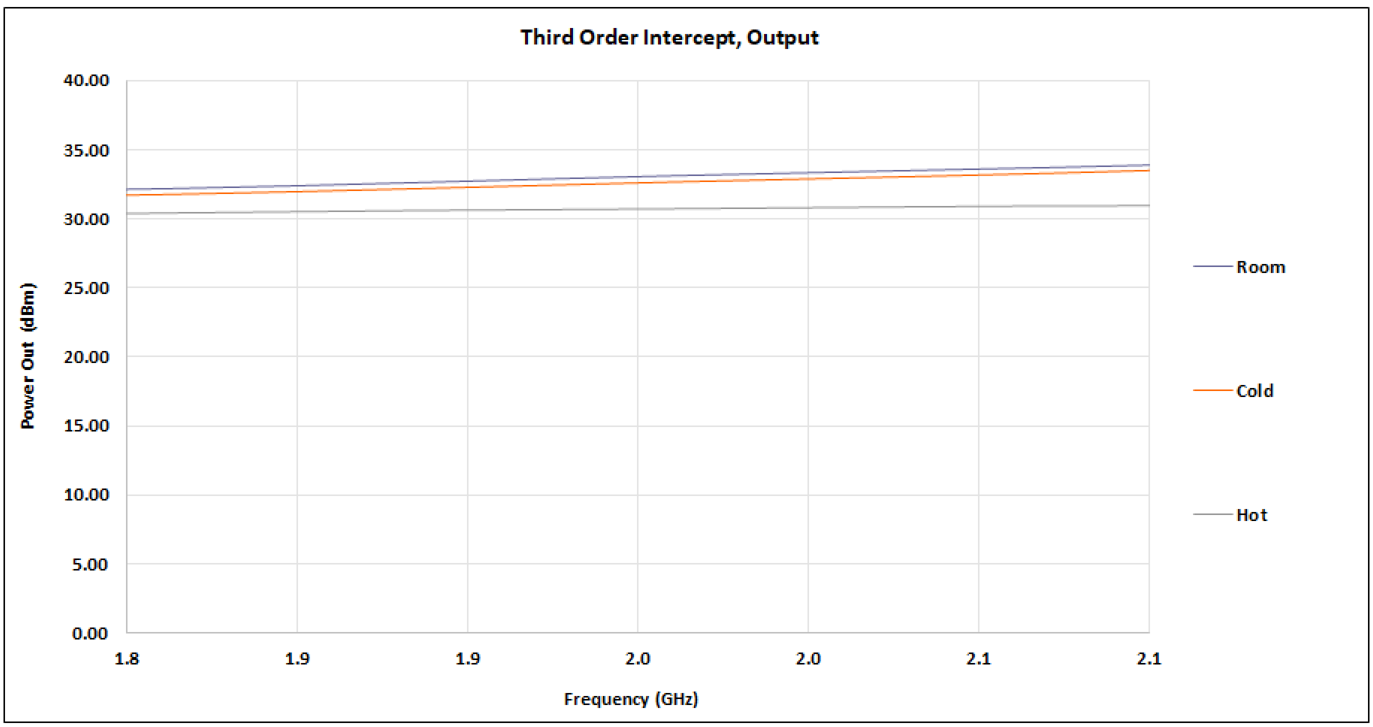




11.0 Typical Characteristics (continued)

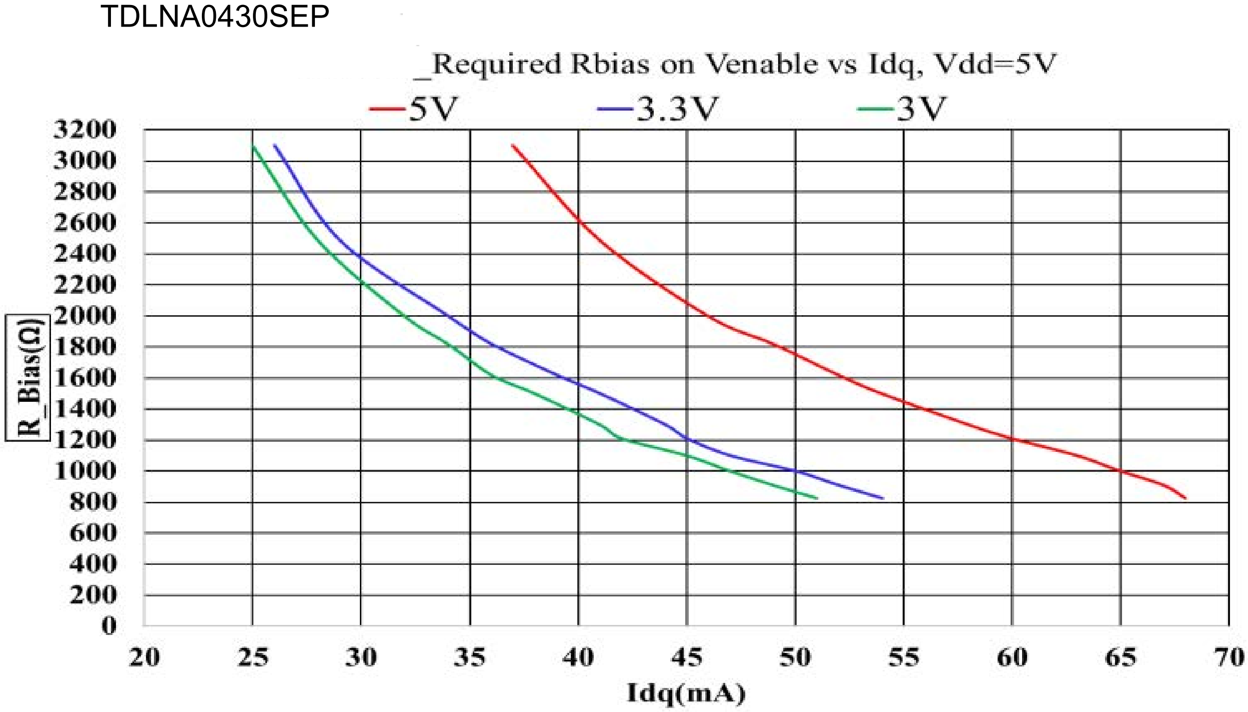
Test Conditions: Vdd = 5 V, Cold = -55 ºC, Room = 25 ºC, Hot = 125 ºC





11.0 Typical Characteristics (continued)

Test Conditions: As noted @ Room = 25 ºC



Rbias on Venable vs Idq

12.0 Test Procedures

Biasing Sequence

To properly bias the TDLNA0430-EVB-A, follow these steps: Connect the supply Ground the Ground test point.

- Apply bias to the Venable = 5 V test points.
- Apply bias to the Vdd = 5 V test point.
- Apply an RF input signal.

The TDLNA0430-EVB-A is shipped fully assembled and tested. Figure 12.1 illustrates a basic test setup diagram for evaluating s-parameters, which includes gain, input output return loss and reverse isolation using a network analyzer. Follow these steps to complete the test setup and verify the operation of the TDLNA0430-EVB-A

1. Connect the Ground test point to the ground terminal of the power supply.
2. Connect the Venable and Vdd test points to the voltage output terminal of a 5 V supply that sources a current of approximately 60 mA.
3. Connect a calibrated network analyzer to the RF-in, and RF-out SMA connectors. Sweep the frequency from 1 GHz to 6 GHz and set the power to -25 dBm.

The TDLNA0430-EVB-A is expected to have a gain of 21.5 dB at 1.8 GHz. Refer to Table 9.1 for the expected results.Additional test equipment is required for a comprehensive evaluation of the device's functions and performance.

For noise figure evaluation, use either a noise figure analyzer or a spectrum analyzer with a noise option. It is recommended to use a low excess noise ratio (ENR) noise source.
For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is recommended.
For power compression and power handling evaluations, use a two-channel power meter and a signal generator. Ensure that the input power amplifier has sufficient power capacity. Test accessories such as couplers and attenuators must also have adequate power handling capabilities.

Please note that measurements conducted at the SMA connectors of the TDLNA0430-EVB-A include the losses of the SMA connectors and the PCB. The through line should be measured to calibrate the effects of the TDLNA0430-EVB-A. The through line consists of an RF input line and an RF output line that are connected to the device and have equal lengths.

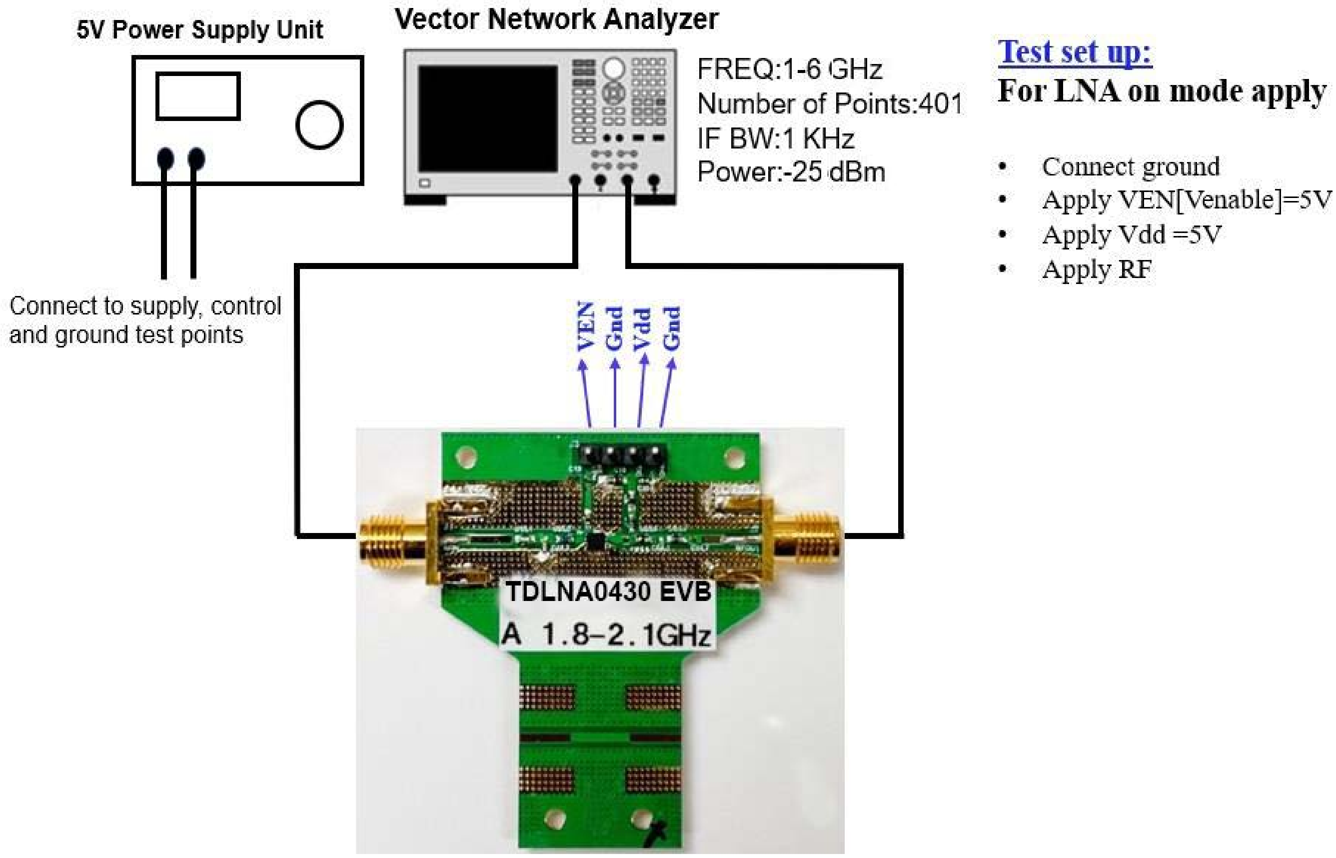
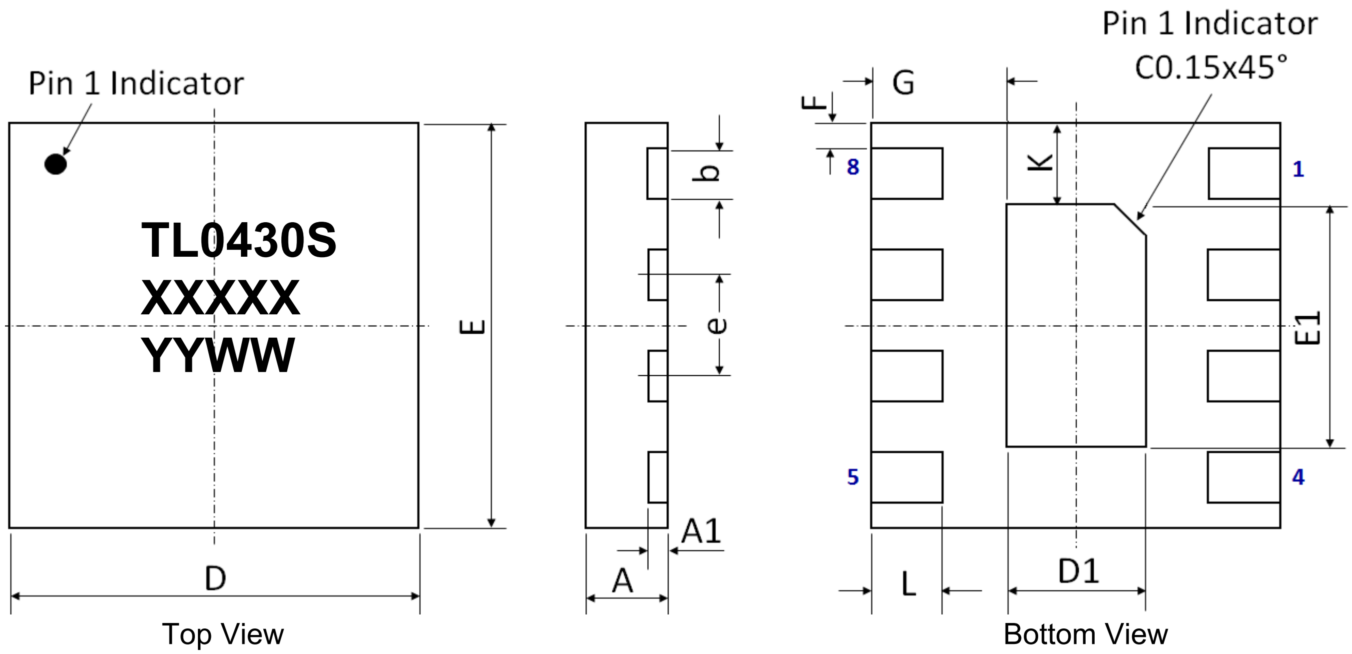


Figure 12.1 TEST Set Up Diagram

13.0 Device Package Information



XXXXX=Lot Mfg Code
YYWW=Date Code

Figure 13.1 Device Package Drawing
(All dimensions are in mm)
Not to scale

Table 13.1 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.75	±0.05	E	2.00 BSC	±0.05
A1	0.203	±0.02	E1	1.20	±0.05
b	0.25	±0.02	F	0.125	±0.02
D	2.00 BSC	±0.05	G	0.66	±0.03
D1	0.68	±0.03	L	0.35	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5 µm ~ 20 µm (Typical 10 µm ~ 12 µm)

14.0 PCB Land Design

Guidelines:
[1] 2-layer PCB is recommended
[2] Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias
[3] Thermal vias shall only be placed on the center pad and should be filled/plugged with solder or copper
[4] The maximum via number for the center pad is 1(X)×2(Y)=2

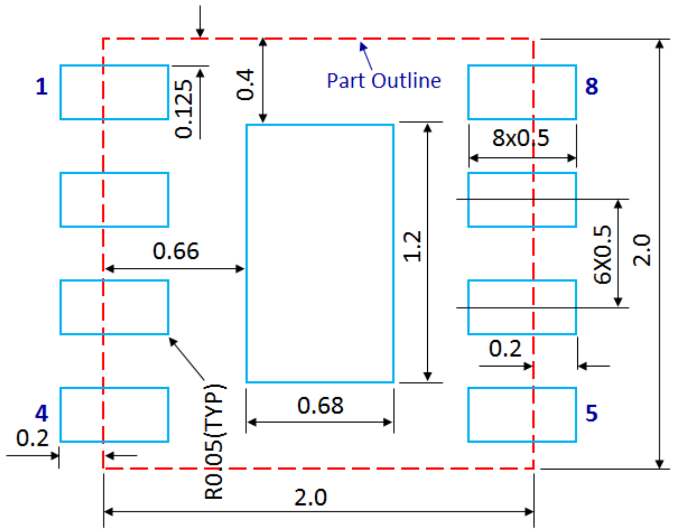


Figure 14.1 PCB Land Pattern
(Dimensions are in mm)

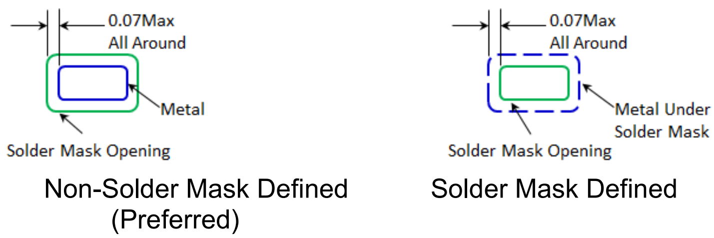
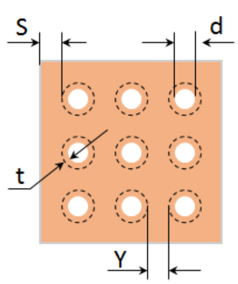


Figure 14.2 Solder Mask Pattern
(Dimensions are in mm)



Not to scale.

Figure 14.3 Thermal Via Pattern
(Recommended Values: S≥0.15 mm; Y≥0.20 mm; d=0.3 mm; Plating Thickness t=25 µm or 50 µm)

15.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125 μm.

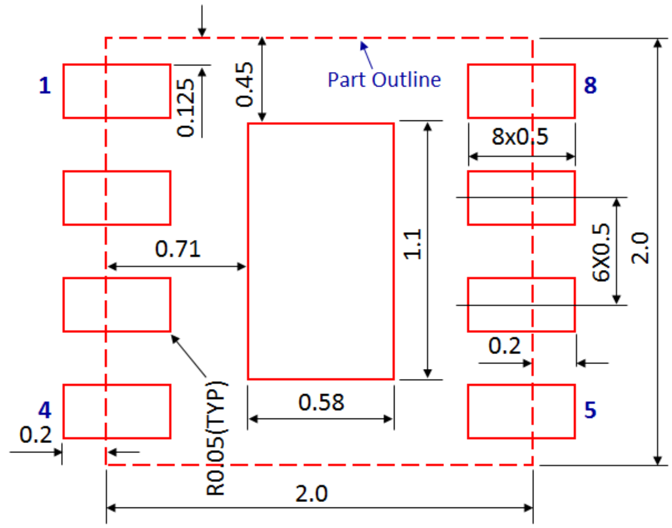


Figure 15.1 Stencil Openings
(Dimensions are in mm)

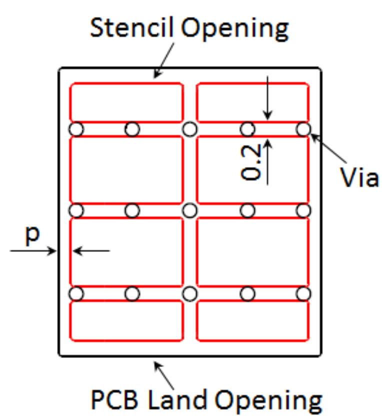


Figure 15.2 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

Not to scale.

Revision Information

Document	Description	Change/Revision Details / Date
TDLNA0430SEP_Prod_Spec	Initial Release of the Product Specification data sheet	Rev 0.1 / 12_27_2023

Document Category Definitions:

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Teledyne e2v HiRel Electronics reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Teledyne e2v HiRel Electronics decides to change the specifications, Teledyne e2v HiRel Electronics will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, Email us at: **hirel@teledyne.com** **website: www.tdehirel.com**

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