# TDPA6005QFN

## X-Band 31.5 dBm Mid-Power Amplifier

### Product Overview

The TDPA6005QFN is a mid-power amplifier, monolithic circuit, which integrates two stages and produces 31.5 dBm output power associated to a high power added efficiency of 33%.

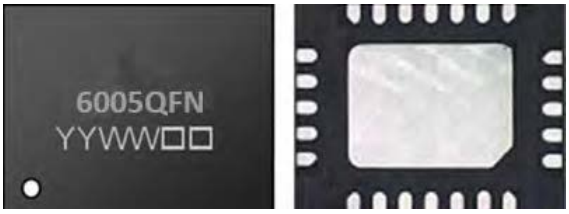
It is designed for a wide range of applications, from professional to commercial communication systems.

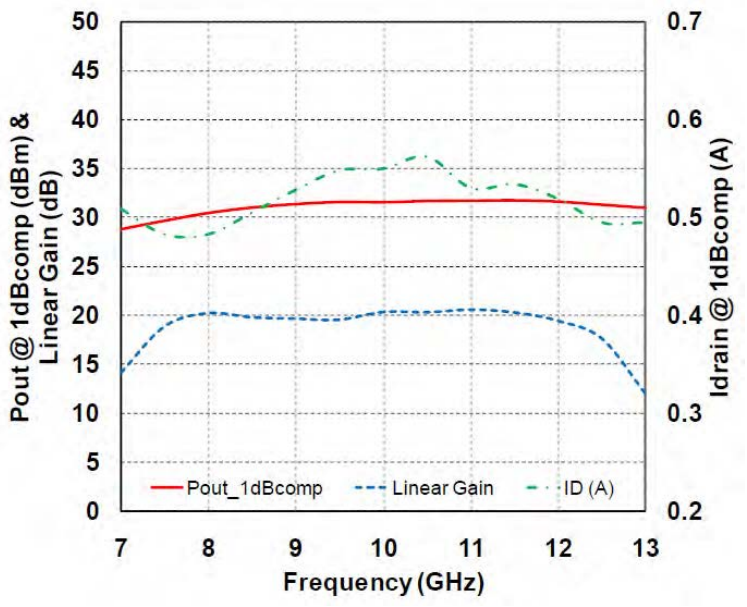
The circuit is manufactured with a pHEMT process, 0.25 µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in a RoHS compliant SMD package.

### Features

- Power: 31.5 dBm
- High PAE: 33%
- Frequency band: 8-12 GHz
- Linear gain: 20 dB
- dc bias: VD = 8 Volt @ Id = 420 mA
- 24-pin, QFN 4 mm x 5 mm
- MSL3

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## Absolute Maximum Ratings[1]

Tamb.= +25°C

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| VD | Drain bias voltage | 9.0 | V |
| Id | Drain bias current | 700 | mA |
| VG | Gate bias voltage | -0.25 | V |
| Pin | Maximum peak input power overdrive | +18 | dBm |
| Tj | Junction temperature | 175 | °C |
| Ta | Operating temperature range | -40 to +85 | °C |
| Tstg | Storage temperature range | -55 to +150 | °C |

(1) Operation of this device above anyone of these parameters may cause permanent damage.

## Electrical Characteristics

Tamb.= +25°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Freq | Frequency range | 8 | | 12 | GHz |
| G | Linear Gain | | 20 | | dB |
| P1dB | Output Power@ 1 dB comp. | | 31.5 | | dBm |
| PAE1dB | Power Added Efficiency @ 1 dB comp. | | 33 | | % |

ESD Protection: Electrostatic discharge sensitive device, please observe handling precautions!

## Electrical Specifications (Pulsed Mode)

Tamb.= +25°C, VD1,2 = +8.0V

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Freq | Operating frequency | 8 | | 12 | GHz |
| G | Small signal gain | | 19.5 | | dB |
| RIin | Input Return Loss | | 14 | | dB |
| RIout | Output Return Loss | | 10 | | dB |
| P1d8 | Output power @ 1 dBcomp | | 31.5 | | dBm |
| P3d8 | Output power @ 3 dBcomp | | 32 | | dBm |
| PAE1dB | Power Added Efficiency@ 1 dBcomp | | 33 | | % |
| PAE3dB | Power Added Efficiency@3 dBcomp | | 35 | | % |
| Id 1d8comp | Supply drain current@ 1 dBcomp | | 500 | | mA |
| Id 3d8comp | Supply drain current @ 3 dBcomp | | 550 | | mA |
| Idq | Supply quiescent current | | 420 | | mA |
| VG | Gate supply voltage | | -0.7 | | V |

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 nH to 0.3 nH.

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## Typical Bias Conditions

Tamb.= +25°C

| Symbol | Pad N° | Parameter | Values | Unit |
|---|---|---|---|---|
| VD1,2 | 17, 13 | Drain supply voltage | 8 | V |
| VG12 | 18 | Gate supply voltage | -0.7 | V |

## Device Thermal Information

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

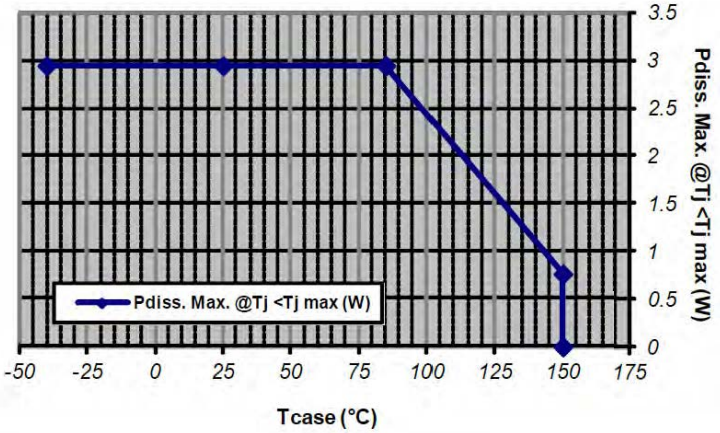
A derating must be applied on the dissipated power if the Tcase temperature cannot be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

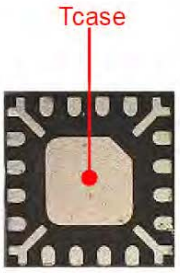
| DEVICE THERMAL SPECIFICATION : CHA6005-QEG | | |
|---|---|---|
| Recommended max. junction temperature (Tj max) | : | 173 °C |
| Tj absolute maximum rating for 20 years minimum life time | : | 175 °C |
| Max. continuous dissipated power (Pdiss. Max.) | : | 2.9 W |
| => Pdiss. Max. derating above Tcase(1)= 85 °C | : | 33 mW/°C |
| Junction-Case thermal resistance (Rth J-C)(2) | : | <30 °C/W |
| Minimum Tcase operating temperature(3) | : | -40 °C |
| Maximum Tcase operating temperature(3) | : | 85 °C |
| Minimum storage temperature | : | -55 °C |
| Maximum storage temperature | : | 150 °C |

*(1) Derating at junction temperature constant = Tj max.*

*(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.*

*(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).*



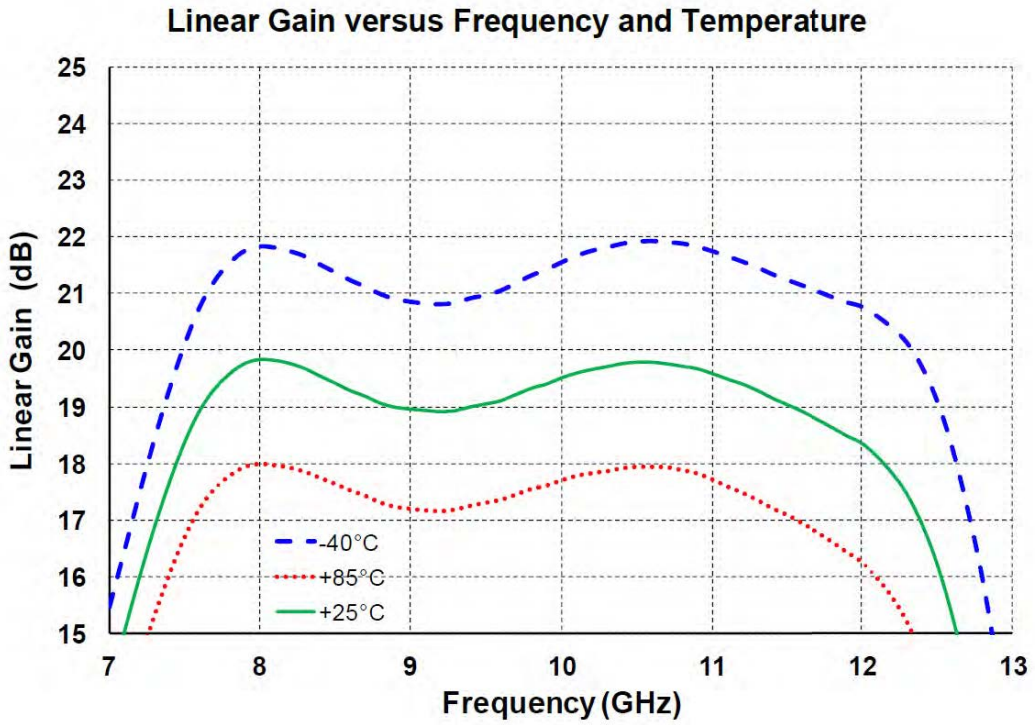



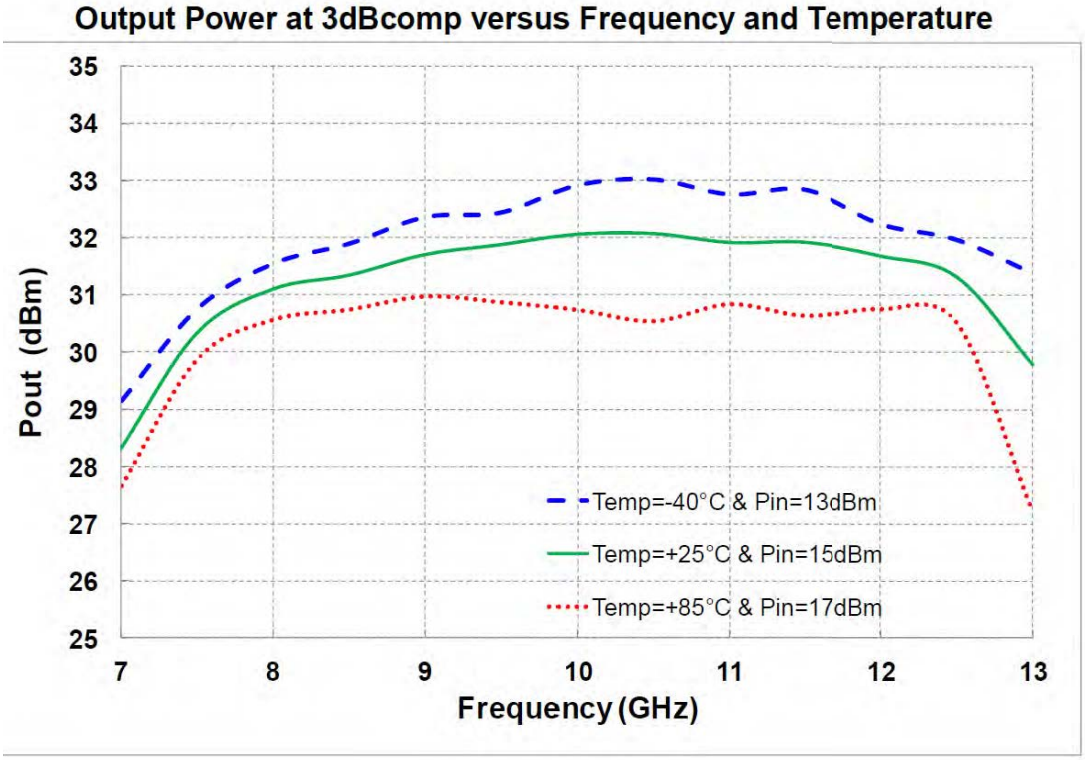

Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.4

## Typical Board Measurements

Temperature: -40, +25, +85 °C, VD1,2 = 8 V,,Id (Quiescent) = 420 mA, CW mode

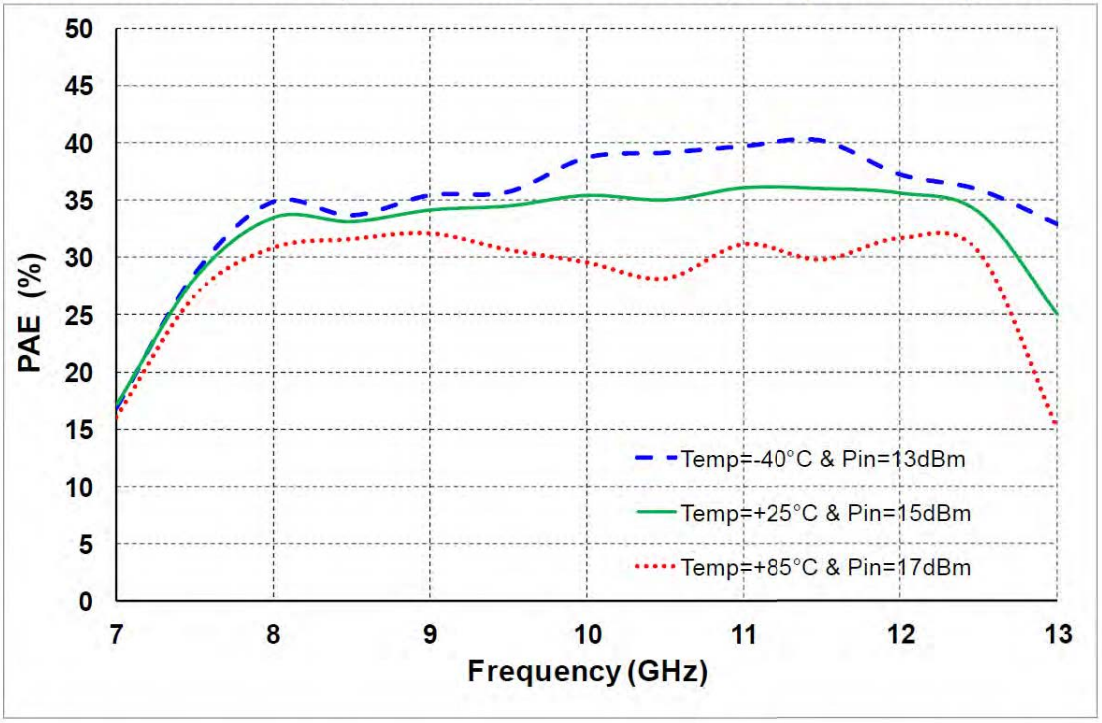


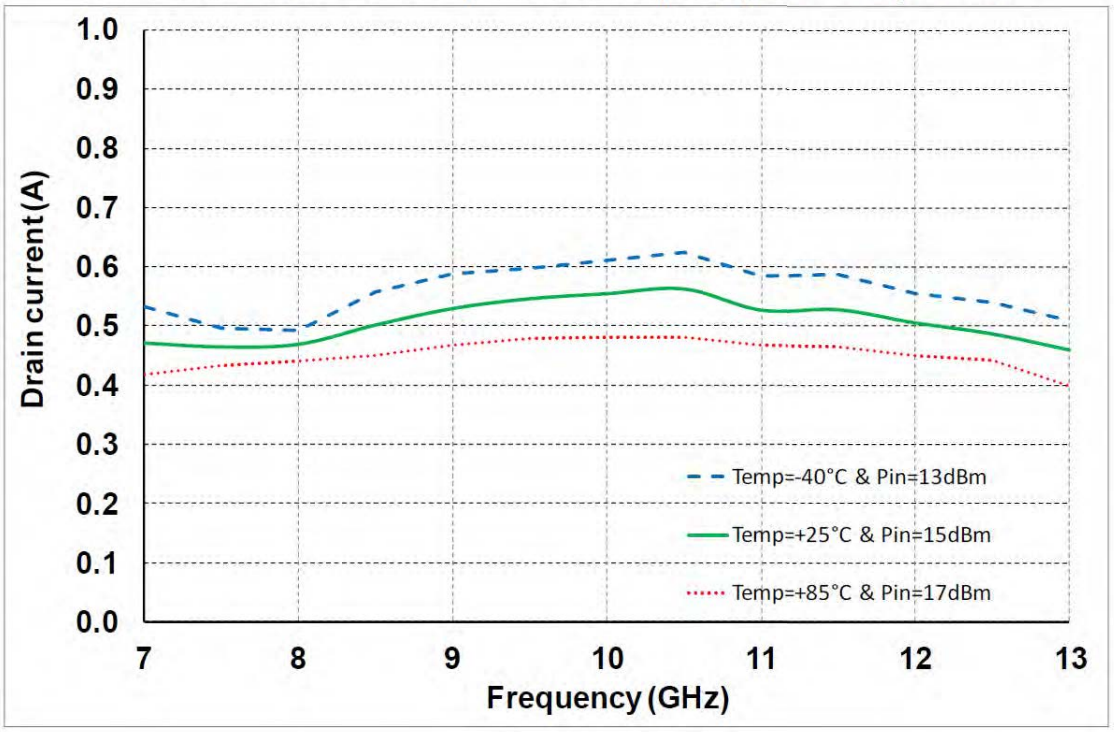
## Typical Board Measurements

Temperature: -40, +25, +85 °C, VD1,2 = 8 V,,Id (Quiescent) = 420 mA, CW mode

**Power added efficiency at 3dBcomp versus Frequency and Temperature**



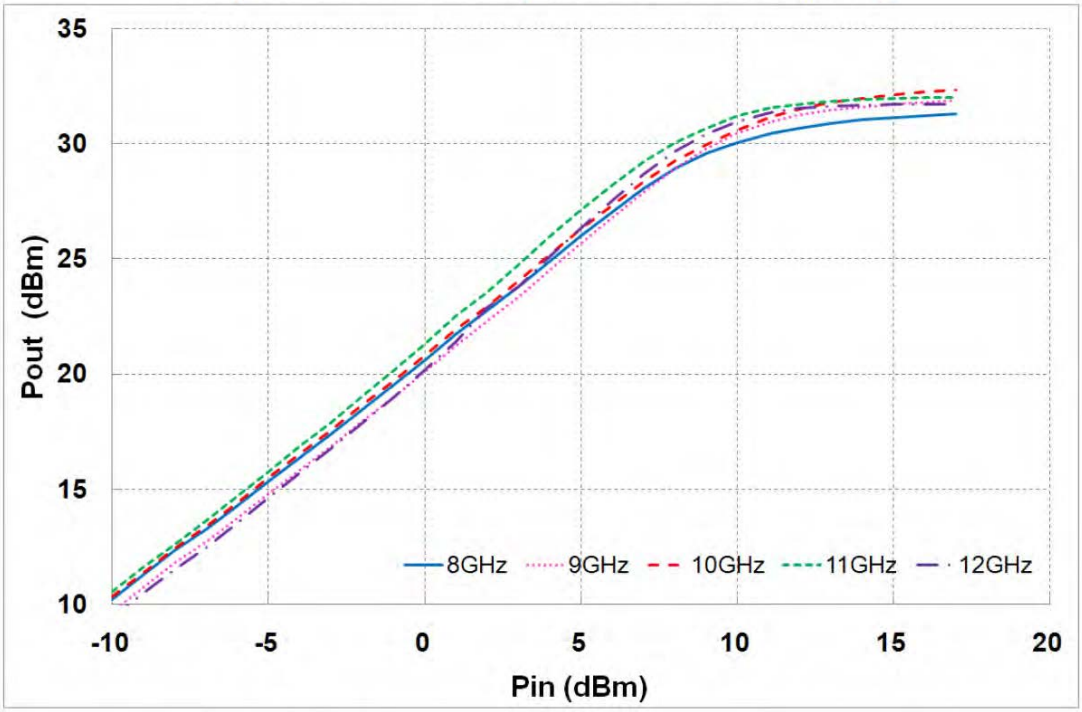

**Drain current at 3 dBcomp versus Frequency and Temperature**



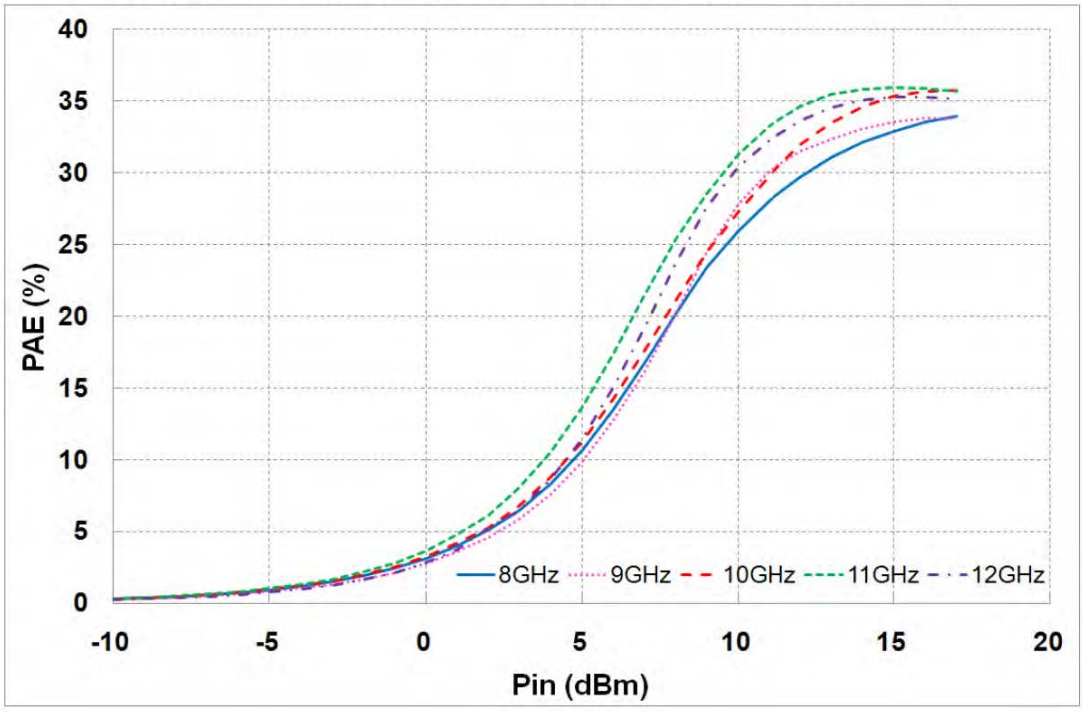
## Typical Board Measurements

Temperature: +25 °C, VD1,2 = 8 V,Id (Quiescent) = 420 mA, CW mode

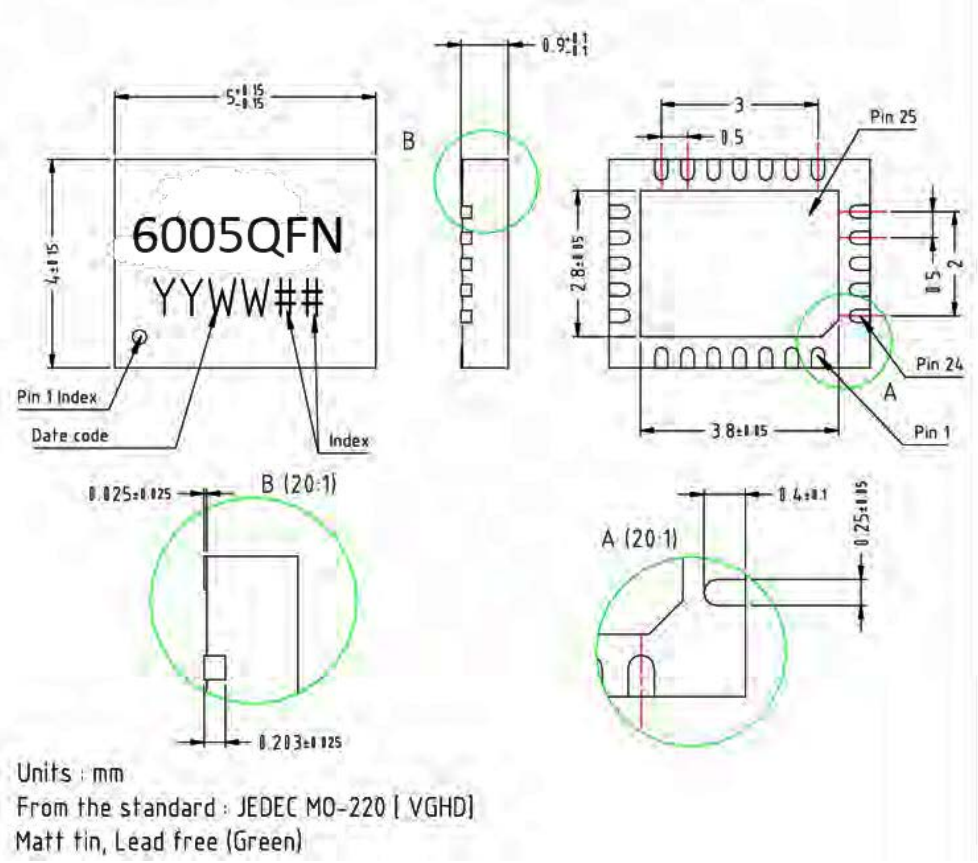
**Output Power versus Input Power and Frequency**




**Power added efficiency versus Input Power and Frequency**



## Package Outline [1]

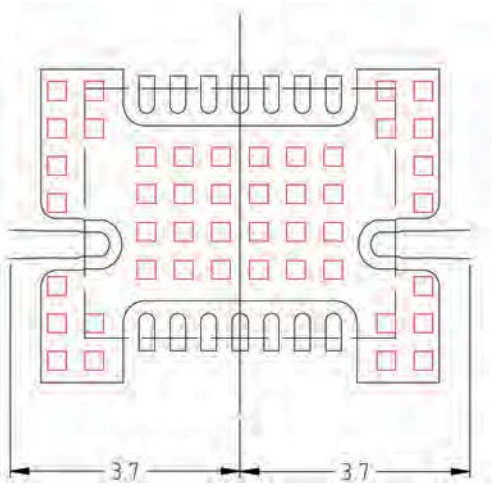



| | | | |
|---|---|---|---|
| Matt tin, Lead Free (Green) | | 1- Ne | 13- VD2 |
| Units: mm | | 2- Ne | 14- Ne |
| From the standard : JEDEC MO-220 (VGHD) | | 3- Ne | 15- Gnd (2) |
| | | 4- Ne | 16- Ne |
| 25- GND | | 5- Ne | 17- VD1 |
| | | 6- Ne | 18- VG1 |
| | | 7- Ne | 19- Ne |
| | | 8- Ne | 20- Ne |
| | | 9- Gnd[1] | 21- Gnd[1] |
| | | 10- RF OUT | 22- RFIN |
| | | 11- Gnd[1] | 23- Gnd[1] |
| | | 12- Ne | 24- Ne |

(1)It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

## Definition of the Reference Planes

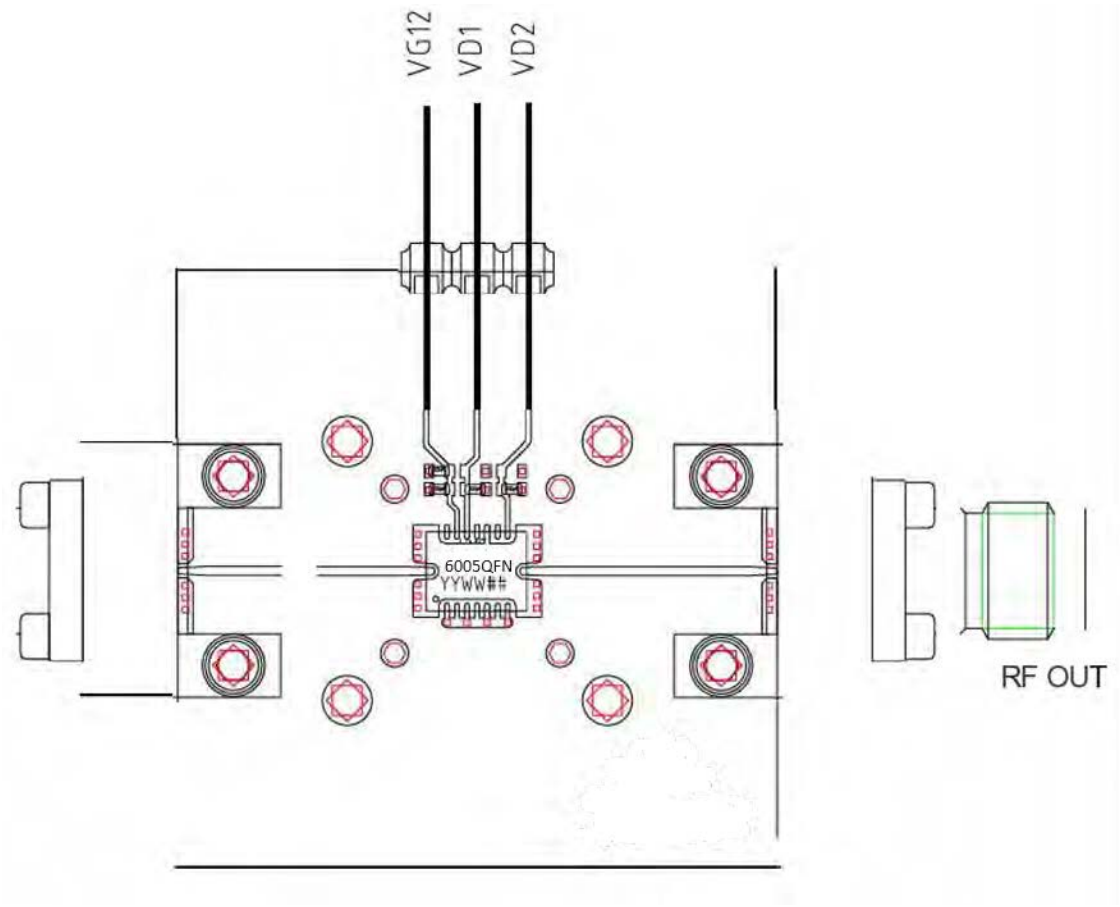
The reference planes used for measurements given above are symmetrical from the axis of the package (see drawing beside). The input and output reference planes are located at 3.7 mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



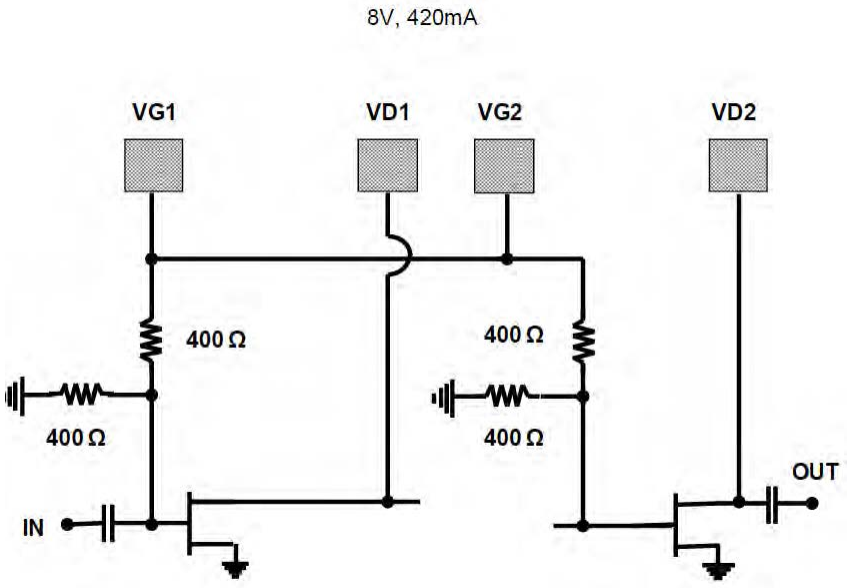
## Evaluation Motherboard

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8 mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100 pF + 10nF recommended on VG12, VD1,2 in CW mode.
- Decoupling capacitors of 100 pF + 10nF recommended on VG12 in pulsed drain mode.
- Decoupling capacitors of 100 pF + 10nF recommended on VD1,2 in pulsed drain mode.
- See application note AN0017 for details.

**Recommended Test fixture for measurements over temperature range**



## DC Schematic




## Package Information

| Parameter | Value |
|---|---|
| Package body material | RoHS-compliant |
| | Low stress Injection Molded Plastic |
| Lead finish | 100% matte tin ( Sn) |
| MSL Rating | MSL3 |

## Ordering Information

| Order Code | Description | Package | Shipping Method |
|---|---|---|---|
| TDPA6005QFN | 5W X Band Medium Power Amplifier | 6 x 6 Ceramic QFN | Tape and Reel |

## Revision Information

| Document | Description / Date | Change/Revision Details |
|---|---|---|
| TDPA6005QFN-4-2024 Rev 0.2 | TDPA6005QFN / April 2024 | Initial Release |

## Document Categories and Definitions:

### Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Teledyne e2v HiRel Electronics reserves the right to change specifications at any time without notice in order to supply the best possible product.

### Product Specification

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